MB61
IDTV
SERVICE MANUAL

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1. INTRODUCTION

17MB61 mainboard is driven by MSD9WB7GX-LF-2. This IC is capable of handling Video and audio processing, Scaling-Display processing, 3D comb filter, OSD and text processing, LVDS transmitting, channel and MPEG2/4 decoding.

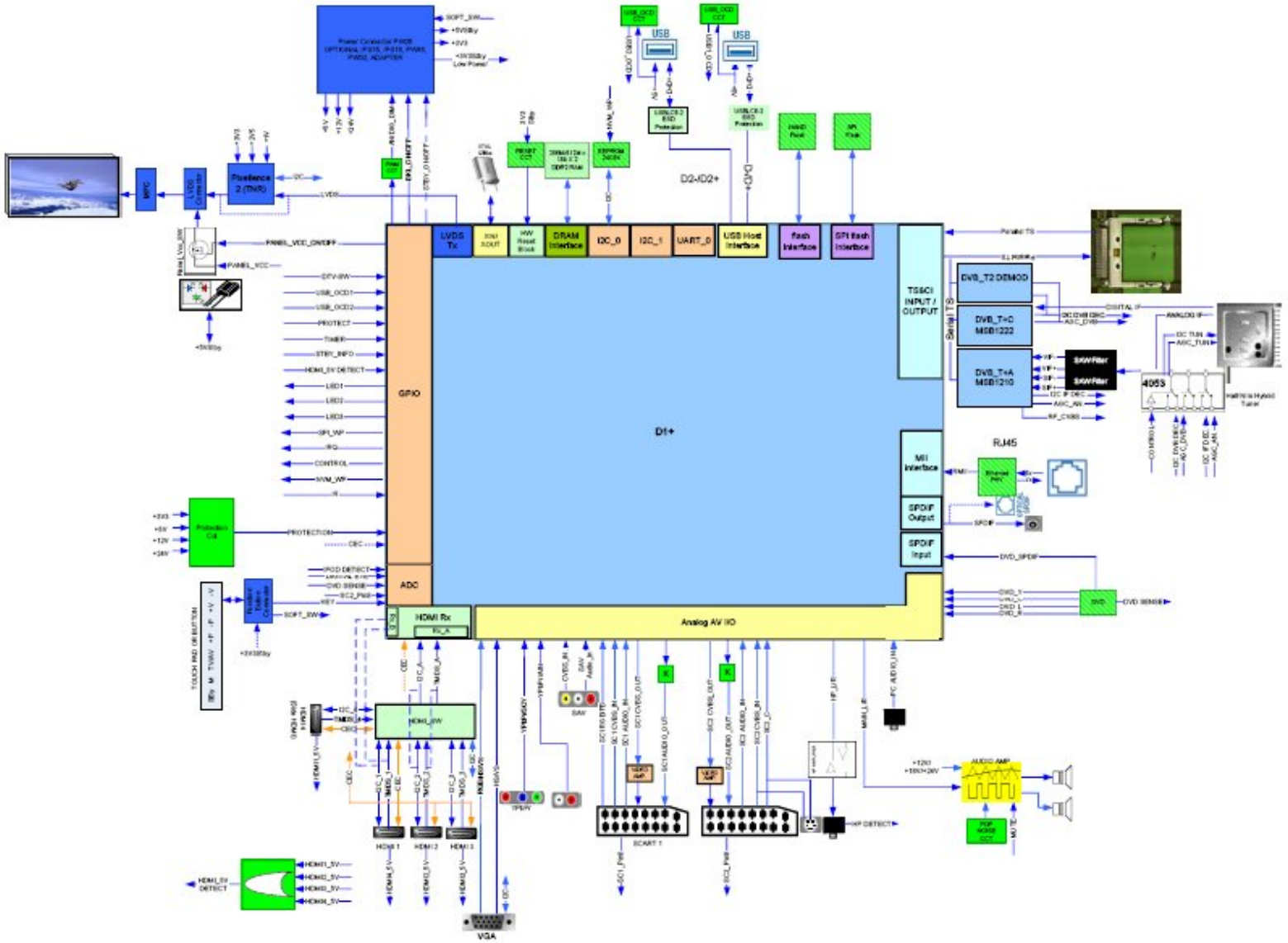
TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Also DVB T, DVB-C are supported external demodulators.

Sound system output is supplying max. 2x8W (10%THD) for stereo 8Ω speakers.

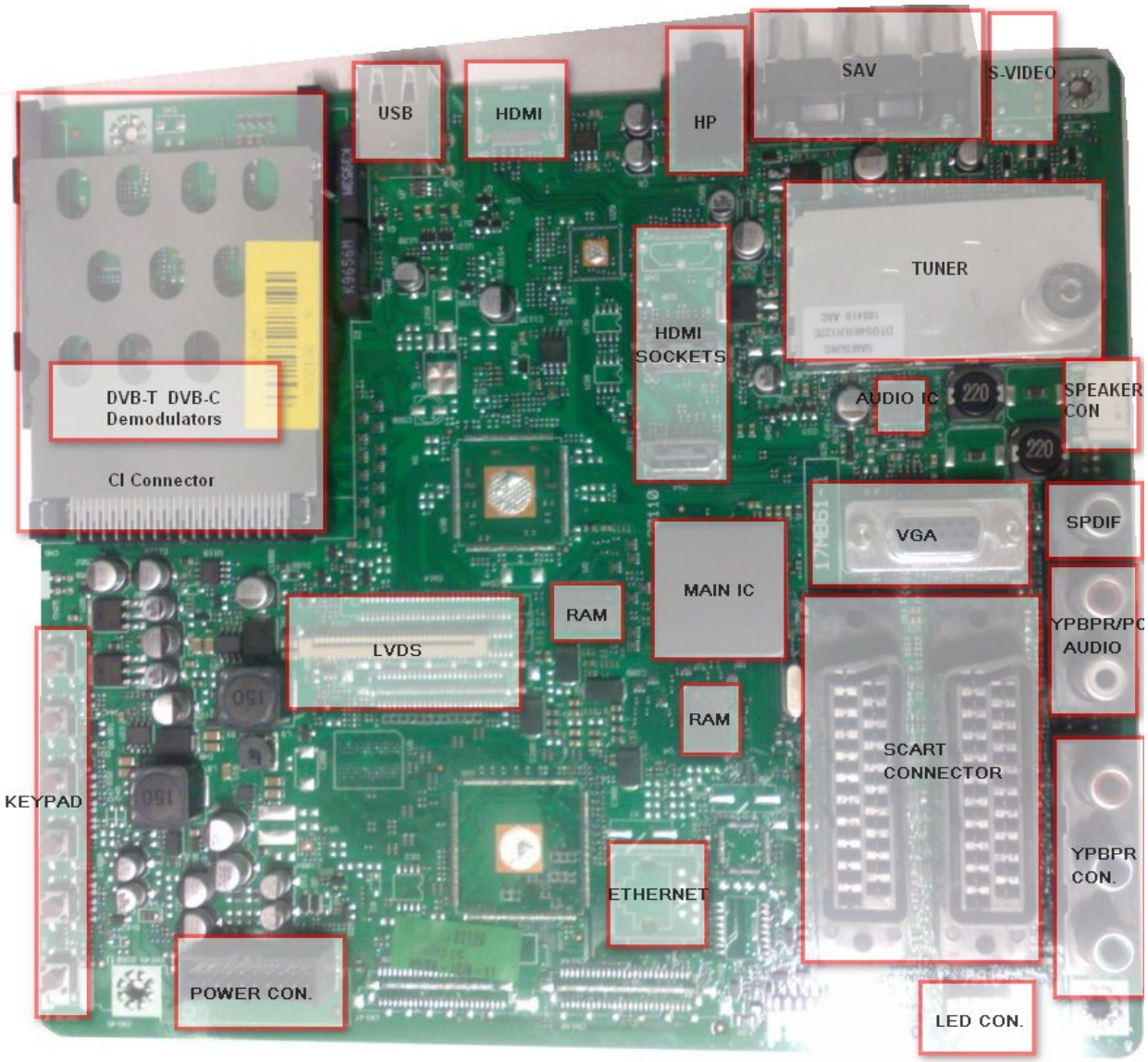
Supported peripherals are:

1 RF input VHF I, VHF III, UHF @ 75Ohm(Common)
1 Side AV (CVBS, R/L_Audio)
2 SCART socket(Common)
1 YPbPr (Common)
1 PC input(Common)
4 HDMI 1.3 input(2 HDMI inputs are common, 4 inputs are optional)
1 S/PDIF output(Common)
1 Headphone(Common)
1 Common interface(Common)
2 USB(Common)
1 DVD(Optional)
1 On-board Keypad(Optional)
1 External Keypad(Optional)
1 External TouchPad(Optional)

1.1. General Block Diagram



1.2. MB61 Placement of Blocks

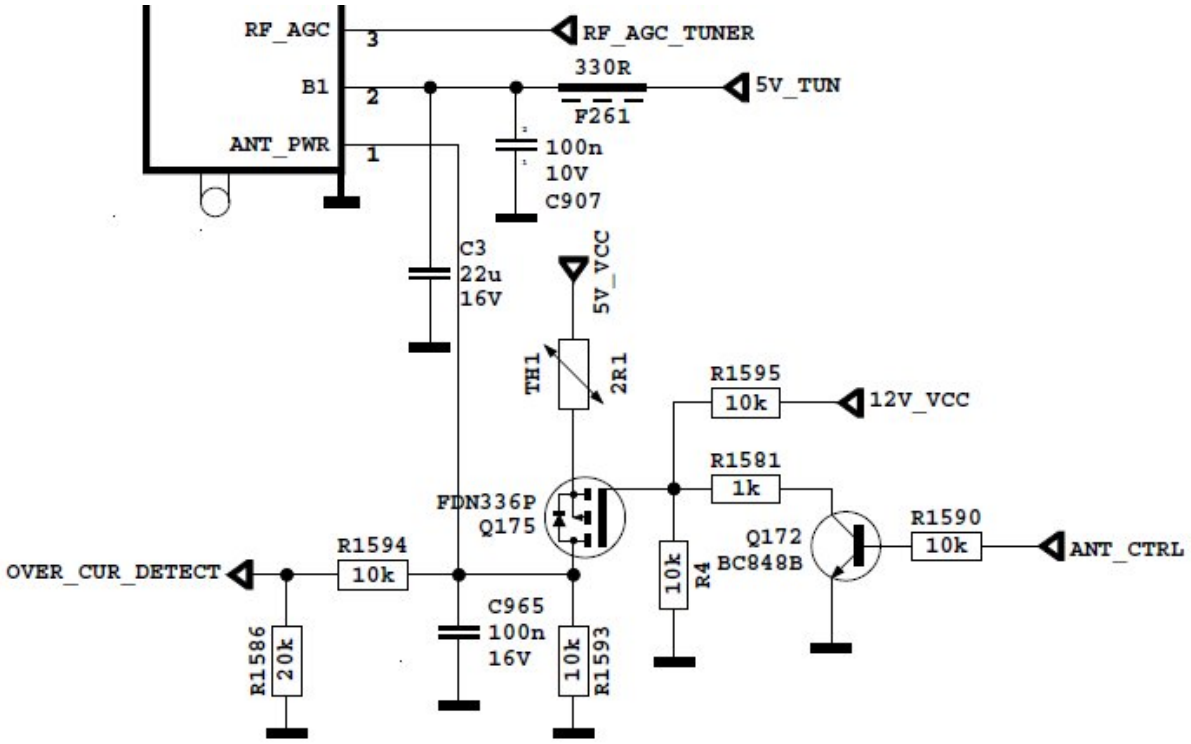


1. TUNER(TU102)

A horizontal mounted and Digital Half-Nim tuner is used in the product, which covers 3 Bands(From 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info about the tuner.

In active antenna option, the following circuit are used. ANT_CTRL pin is controlled by microcontroller. If ANT_CTRL is low, ANT_PWR will be low. If ANT_CTRL is high, ANT_PWR will be high.

OVER_CUR_DETECT pin is a monitor for short circuit in antenna. OVER_CUR_DETECT is low, ANT_CTRL will be low, so ANT_PWR will be low. Finally, short circuit protection is done by circuits and microcontroller.



1.1. General description of Samsung DTOS403LH121B:

The Tuner covers 3 Bands(from 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). Band selection and Tuning are performed digitally via the I2C bus.

1.2. Features of DTOS403LH121B:

- Receiving System: This TUNER is designed to cover the air channels in VHF and UHF, compliant with DVB-T standard. and It covers all Analog channels from 48.25MHz to 863.25MHz
- Receiving Channel (Digital, Center frequency):
  VHF Low CH. E2 ~ S10 (50.5MHz ~ 170.5MHz)
  VHF High CH. E5 ~ S41 (177.5MHz ~ 466 MHz)

UHF CH. E21 ~ E69 (474 MHz ~ 858 MHz)

- Receiving Channel (PAL, Picture carrier frequency):
  VHF Low CH. E2 ~ S10 (48.25MHz ~ 168.25MHz)
  VHF High CH. E5 ~ S41 (175.25MHz ~ 463.25MHz)
  UHF CH. E21 ~ E70 (471.25MHz ~ 863.25MHz)
- Intermediate Frequency:
  Digital(center) DVB-T (36.167 MHz)
  Digital(center) DVB-C (36.125 MHz)
  Analog(picture) 38.9 MHz
- Input Impedance: 75Ω, Unbalanced
- Band Change-Over System
  PLL Control System
- Tuning System
  Electronic Tuning System With PLL
- Internal(or External) RF AGC function
  Built in wideband AGC detector with 6 programmable take-over points

1.3. Pinning:

Pin no.	Terminal Name	Pin Description
1	Ant Power	Active Antenna Power
2	B+	+5V, Supply Voltage (Preamplifier, DC/DC)
3	RF AGC	RF AGC (internal or external mode)
4	CL	I2C Serial Clock
5	DA	I2C Serial Clock
6	BP	+5V, Supply Voltage (RF Amp, PLL, IF Amp)
7	BT(T.P)	+33V, within DC/DC circuit
8	AS	I2C Address Selection of the PLL
9	IF AGC	Control voltage for the IF AGC
10	IF OUT +	Output 2 of the IF Amplifier
11	IF OUT -	Output 1 of the IF Amplifier
12	AIF Output	IF output of the Analog BroadBand

2. SAW FILTER – Audio – Epcos K9656M(Z101)

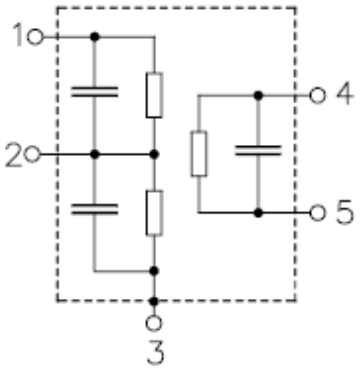
2.1. Standart

- B/G
- D/K
- I
- L/L’

2.2. Features

- TV IF audio filter with two channels
- Channel 1 (L’) with one pass band for sound carriers at 40,40 MHz (L’) and 39,75 MHz (L’-NICAM)
- Channel 2 (B/G,D/K,L,I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

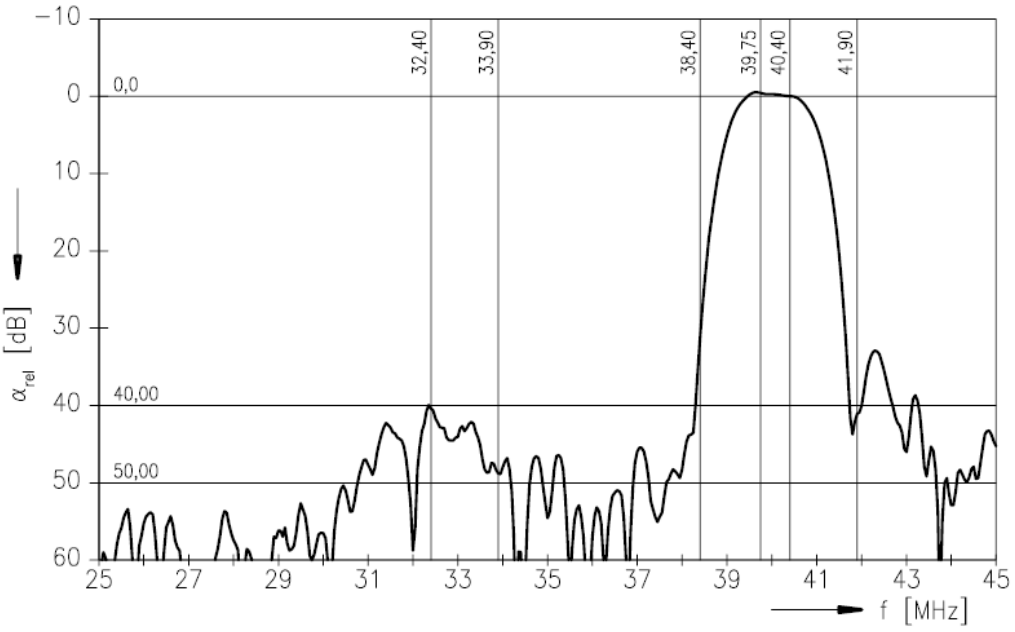
2.3. Pin configuration



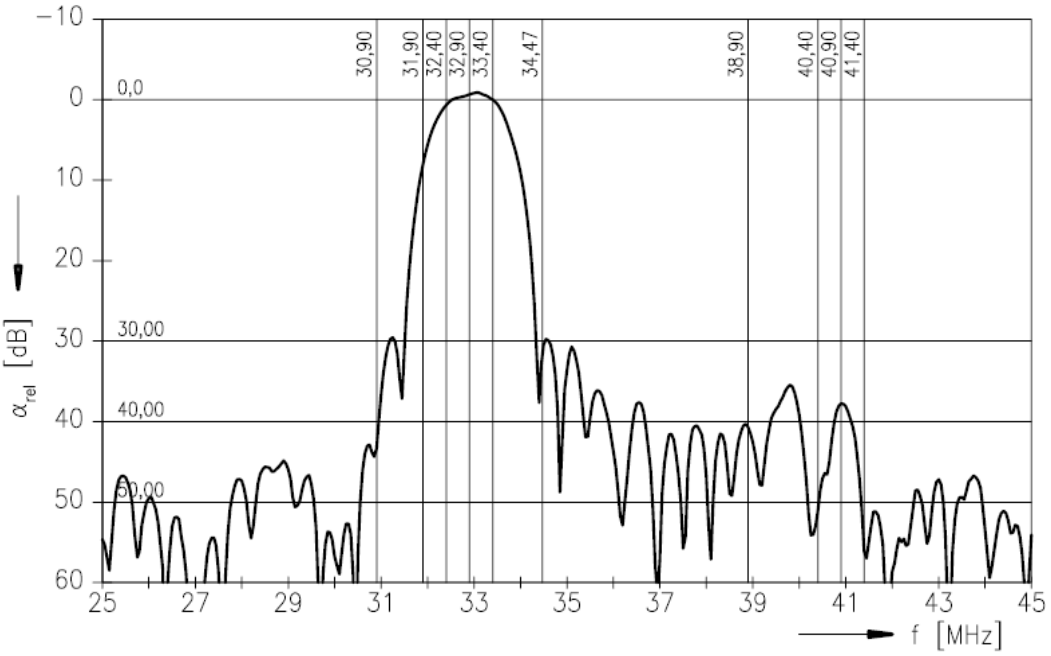
1 Input
2 Switching input
3 Chip carrier - ground
4 Output
5 Output

2.4. Frequency response

Frequency response of channel 1



Frequency response of channel 2



3. SAW FILTER – Video – Epcos K3958M(Z102)

3.1. Standart

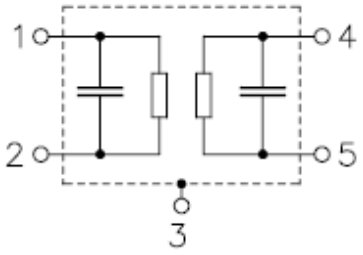
- B/G
- D/K
- I
- L/L'

3.2. Features

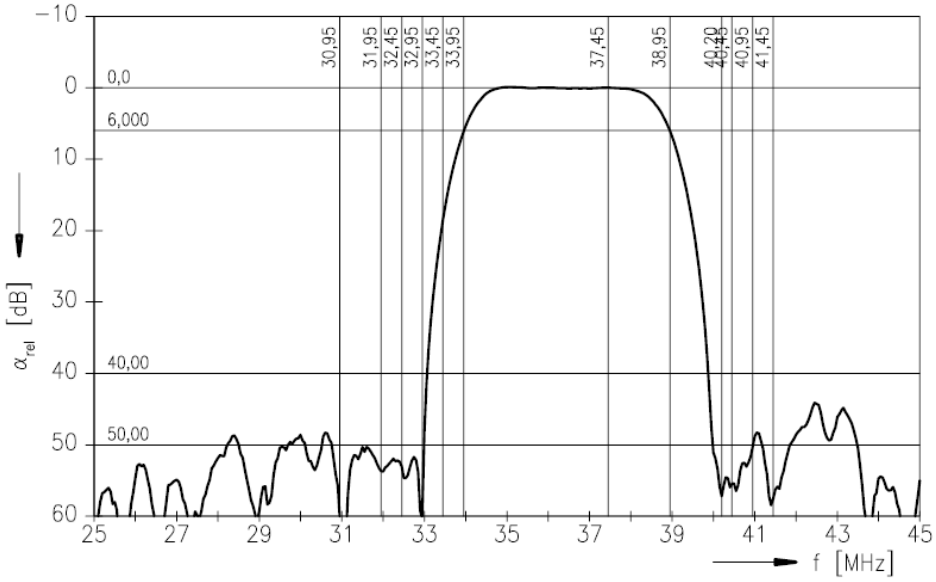
- TV IF filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

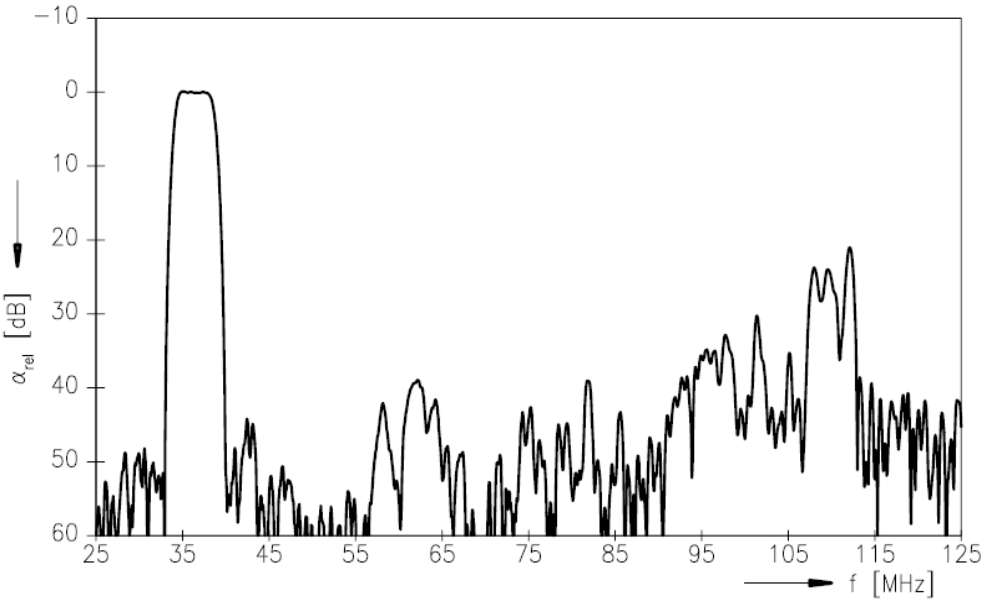
Pin configuration:

1 Input
2 Input - ground
3 Chip - carrier ground
4 Output
5 Output



3.3. Frequency response





4. AUDIO AMPLIFIER STAGE WITH MAX9736

4.1. General Description

The MAX9736A/B Class D amplifiers provide high-performance, thermally efficient amplifier solutions. The MAX9736A delivers 2 x 15W into 8Ω loads, or 1 x 30W
into a 4Ω load. The MAX9736B delivers 2 x 6W into 8Ω loads or 1 x 12W into a 4Ω load. These devices are pinfor-pin compatible, allowing a single audio design to work across a broad range of platforms, simplifying design efforts, and reducing PCB inventory.
Both devices operate from 8V to 28V and provide a high PSRR, eliminating the need for a regulated power supply. The MAX9736 offers up to 88% efficiency at 12V supply.
Pin-selectable modulation schemes select between filterless modulation and classic PWM modulation. Filterless modulation allows the MAX9736 to pass CE EMI limits with 1m cables using only a low-cost ferrite bead and capacitor on each output. Classic PWM modulation is optimized for best audio performance when using a full LC filter.
A pin-selectable stereo/mono mode allows stereo operation into 8Ω loads or mono operation into 4Ω loads. In mono mode, the right input op amp becomes available
as a spare device, allowing flexibility in system design.
Comprehensive click-and-pop reduction circuitry minimizes noise coming into and out of shutdown or mute. Input op amps allow the user to create summing amplifiers,
lowpass or highpass filters, and select an optimal gain.
The MAX9736A/B are available in 32-pin TQFN packages and specified over the -40°C to +85°C temperature
range.

4.2. Features

Wide 8V to 28V Supply Voltage Range
- **Spread-Spectrum Modulation Enables Low EMI Solution**
- **Passes CE EMI Limits with Low-Cost Ferrite Bead/Capacitor Filter**
- **Low BOM Cost, Pin-for-Pin Compatible Family**
- **High 67dB PSRR at 1kHz Reduces Supply Cost**
- **88% Efficiency Eliminates Heatsink**
- **Thermal and Output Current Protection**
- **< 1µA Shutdown Mode**
- **Mute Function**
- **Space-Saving, 7mm x 7mm x 0.8mm, 32-Pin TQFN Package**

4.3. Absolute Ratings

4.3.1. Electrical Characteristics

(V_{PVDD} = 20V, V_{VS} = 5V, AGND = PGND = 0V, V_{MOD} = $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, REGEN = MONO = AGND, C1 = 0.1µF, C2 = 1µF, $R_{IN\_}$ = 20kΩ and $R_{FB\_}$ = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AMPLIFIER DC CHARACTERISTICS							
Speaker Supply Voltage Range	PVDD	Inferred from PSRR test		8		28	V
Preamplifier Supply Voltage Range	VS	(Notes 1 and 7)		4.5		5.5	V
Undervoltage Lockout	UVLO				7		V
Quiescent Supply Current	I_{PVDD}	R_L = ∞, V_{REGEN} = 5V, V_{VS} = open	T_A = +25°C		30	45	mA
			T_A = T_{MIN} to T_{MAX}			50	
	I_{VS}	R_L = ∞, V_{REGEN} = 0V, V_{VS} = 5V	T_A = +25°C		14	20	mA
			T_A = T_{MIN} to T_{MAX}			22	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V	I_{PVDD}		1	10	µA
			I_{VS}			10	
REG Voltage	V_{REG}				4.2		V
Preregulator Voltage	VS	Internal regulated 5V, V_{REGEN} = 5V			4.8		V
COM Voltage	V_{COM}			1.9	2.05	2.2	V
INPUT AMPLIFIER CHARACTERISTICS							
Capacitive Drive	C_L				30		pF
Output Swing (Note 6)		Sinking ±1mA			±2		V
Open-Loop Gain	A_{VO}	$V_{FB\_}$ = V_{COM} ±500mV, $R_{FB\_}$ = 20kΩ to IN_			88		dB
Input Offset Voltage	V_{OS}				±1		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = 20V, V_{VS} = 5V, AGND = PGND = 0V, V_{MOD} = $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, REGEN = MONO = AGND, C1 = 0.1µF, C2 = 1µF, $R_{IN\_}$ = 20kΩ and $R_{FB\_}$ = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Amplifier Slew Rate						2.5		V/µs
Input Amplifier Unity-Gain Bandwidth						3.5		MHz
AMPLIFIER CHARACTERISTICS								
Output Amplifier Gain (Note 8)	A_V	MAX9736A			16.5	17	17.5	dB
		MAX9736B			13.1	13.6	14.1	
Output Current Limit					3.3	4.6		A
Output Offset	V_{OS}	OUT_+ to OUT_-, T_A = +25°C				±2	±10	mV
Power-Supply Rejection Ratio	PSRR	PVDD = 8V to 28V, T_A = +25°C			65	80		dB
		f = 1kHz, 100mVp-p ripple				67		
MAX9736A Output Power (THD+N = 1%)	$P_{OUT\_1\%}$	PVDD = 12V	Stereo	R_L = 8Ω		6		W
				R_L = 4Ω		13		
			Mono	R_L = 4Ω		15.5		
		PVDD = 16V	Stereo	R_L = 8Ω		13.5		
			Mono	R_L = 4Ω		27		
		PVDD = 24V	Stereo	R_L = 8Ω		13.5		
			Mono	R_L = 4Ω		27		
MAX9736B Output Power (THD+N = 1%)	$P_{OUT\_1\%}$	PVDD = 12V	Stereo	R_L = 8Ω		6		W
				R_L = 4Ω		11		
			Mono	R_L = 4Ω		12		
		PVDD = 16V	Stereo	R_L = 8Ω		6		
			Mono	R_L = 4Ω		12		
		PVDD = 24V	Stereo	R_L = 8Ω		6		
			Mono	R_L = 4Ω		12		
MAX9736A Output Power (THD+N = 10%)	$P_{OUT\_10\%}$	PVDD = 12V	Stereo	R_L = 8Ω		10		W
				R_L = 4Ω		16		
			Mono	R_L = 4Ω		19.5		
		PVDD = 16V	Stereo	R_L = 8Ω		17.5		
			Mono	R_L = 4Ω		35		
		PVDD = 24V	Stereo	R_L = 8Ω		17.5		
			Mono	R_L = 4Ω		35		
MAX9736B Output Power (THD+N = 10%)	$P_{OUT\_10\%}$	PVDD = 12V	Stereo	R_L = 8Ω		7.5		W
				R_L = 4Ω		14		
			Mono	R_L = 4Ω		15		
		PVDD = 16V	Stereo	R_L = 8Ω		7.5		
			Mono	R_L = 4Ω		15		
		PVDD = 24V	Stereo	R_L = 8Ω		7.5		
			Mono	R_L = 4Ω		15		

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = 20V, V_{VS} = 5V, AGND = PGND = 0V, V_{MOD} = $V_{\overline{SHDN}}$ = $V_{\overline{MUTE}}$ = 5V, REGEN = MONO = AGND, C1 = 0.1µF, C2 = 1µF, $R_{IN\_}$ = 20kΩ and $R_{FB\_}$ = 20kΩ, R_L = ∞, AC measurement bandwidth 22Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	MAX9736A, P_{OUT} = 4W, f = 1kHz, PWM modulation mode, R_L = 8Ω			0.04		%
		MAX9736B, P_{OUT} = 2W, f = 1kHz, PWM modulation mode, R_L = 8Ω			0.04		
Signal-to-Noise Ratio	SNR	A-weighted	MAX9736A, P_{OUT} = 8W, R_L = 8Ω		96.5		dB
			MAX9736B, P_{OUT} = 6W, R_L = 8Ω		97		
Noise	V_N	A-weighted (Note 9)	MAX9736A		120		µV_{RMS}
			MAX9736B		100		
Crosstalk		L to R, R to L, P_{OUT} = 1W, f = 1kHz, R_L = 8Ω			100		dB
Efficiency	η	P_{OUT} = 6W, MAX9736A, PVDD = 12V, R_L = 8Ω			88		%
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A-weighted (Notes 9 and 10)	Into mute		36		dBV
			Out of mute		36		
Switching Frequency				270	300	330	kHz
Spread-Spectrum Bandwidth					±4		kHz
Thermal Shutdown Level					160		°C
Thermal Shutdown Hysteresis					30		°C
Turn-On Time	t_{ON}				110		ms
DIGITAL INTERFACE							
Input Voltage High	V_{INH}			2			V
Input Voltage Low	V_{INL}					0.8	V
Input Voltage Hysteresis					50		mV
Input Leakage Current						±10	µA

Note 4: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 5: Stereo mode (MONO = GND) specified with 8Ω resistive load in series with a 68µH inductive load connected across BTL outputs. Mono mode (MONO = 5V) specified with a 4Ω resistive load in series with a 33µH inductive load connected across BTL outputs.

Note 6: Output swing is specified with respect to V_{COM}.

Note 7: For typical applications, an external 5V supply is not required. Therefore, set REGEN = 5V. If thermal performance is a concern, set REGEN = 0V and provide an external regulated 5V supply.

Note 8: Output amplifier gain is defined as:

$$20 \times \log\left(\frac{|(V_{OUT\_+}) - (V_{OUT\_-})|}{|V_{FB\_}|}\right)$$

Note 9: Amplifier inputs AC-coupled to GND.

Note 10: Specified at room temperature with an 8Ω resistive load in series with a 68µH inductive load connected across BTL outputs. Mode transitions controlled by $\overline{SHDN}$ control pin.

4.4. Pinning

PIN	NAME	FUNCTION
1, 2	OUTL-	Left-Channel Negative Speaker Output
3	BOOT	Charge-Pump Output. Connect a 1µF charge-pump holding capacitor from BOOT to PGND.
4	MONO	Mono Select. Set MONO high for mono mode, low for stereo mode.
5	FBL	Left-Channel Feedback. Connect feedback resistor between FBL and INL to set amplifier gain.
6	INL	Stereo Left-Channel Inverting Input. In mono mode, INL is the inverting audio input for the mono amplifier.
7, 8, 17	N.C.	No Connection. Not internally connected. OK to connect to PGND.
9	$\overline{MUTE}$	Mute Input. Drive $\overline{MUTE}$ low to place the device in mute mode.
10	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to place the device in shutdown mode.
11	REGEN	Internal Regulator Enable Input. Connect REGEN to $\overline{SHDN}$ to enable the internal regulator. Drive REGEN low to disable the internal regulator, and supply the device with an external 5V supply on VS. See the *Power-Supply Sequencing* section.
12	COM	Internal 2V Bias. Bypass COM to AGND with a 1µF capacitor.
13, 14	AGND	Analog Ground
15	REG	Internal Regulator Output. Bypass REG to AGND with a 1µF capacitor.
16	VS	5V Regulator Supply. Bypass VS to AGND with a 1µF capacitor. If REGEN is low, the internal regulator is disabled, and an external 5V supply must be connected to VS. See the *Power-Supply Sequencing* section.
18	INR	Stereo Right-Channel Inverting Audio Input. In mono mode, INR is the inverting audio input for the uncommitted preamplifier (see the *Mono Configuration* section for more details).
19	FBR	Right-Channel Feedback. Connect feedback resistor between FBR and INR to set amplifier gain.
20	MOD	Output Modulation Select. Sets the output modulation scheme: V_{MOD} = Low, classic PWM/fixed-frequency mode V_{MOD} = High, filterless modulation/spread-spectrum mode
21	C1N	Charge-Pump Flying-Capacitor Negative Terminal
22	C1P	Charge-Pump Flying-Capacitor Positive Terminal
23, 24	OUTR-	Right-Channel Negative Speaker Output
25, 26	OUTR+	Right-Channel Positive Speaker Output
27, 30	PVDD	Power Supply. Bypass each PVDD pin to ground with 0.1µF capacitors. Also, use a single 220µF capacitor between PVDD and PGND.
28, 29	PGND	Power Ground
31, 32	OUTL+	Left-Channel Positive Speaker Output
—	EP	Exposed Pad. Must be externally connected to PGND.

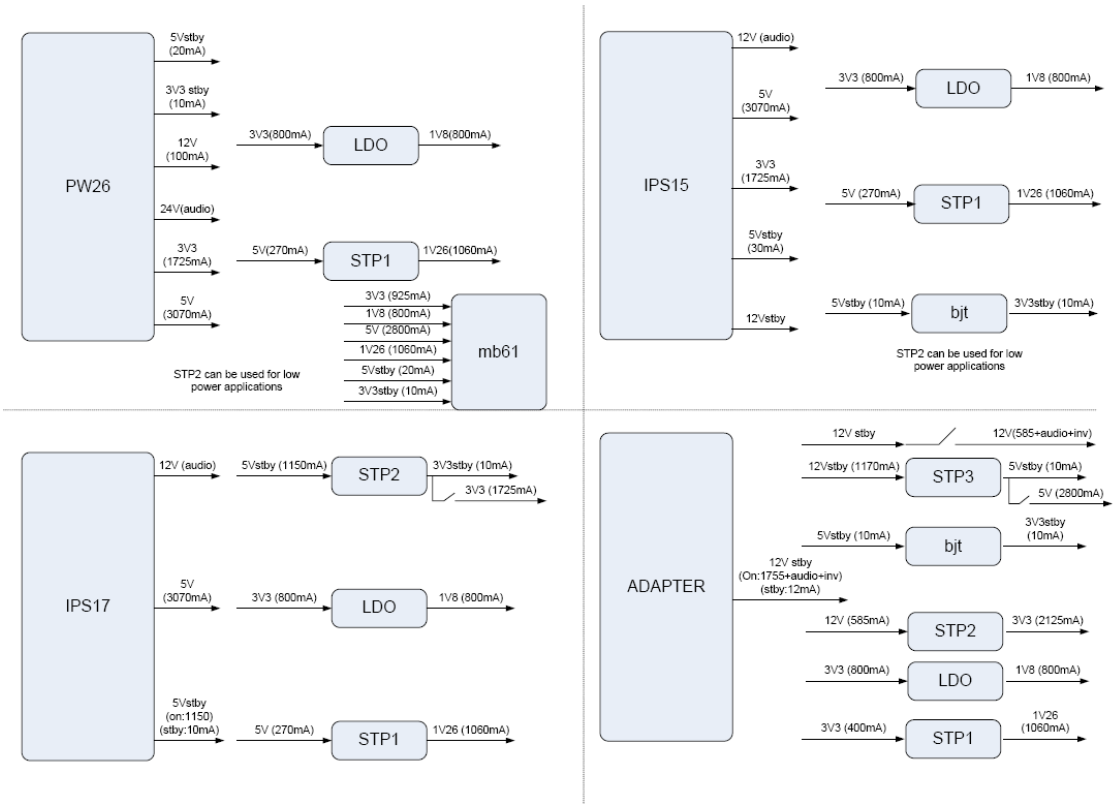
5. POWER STAGE

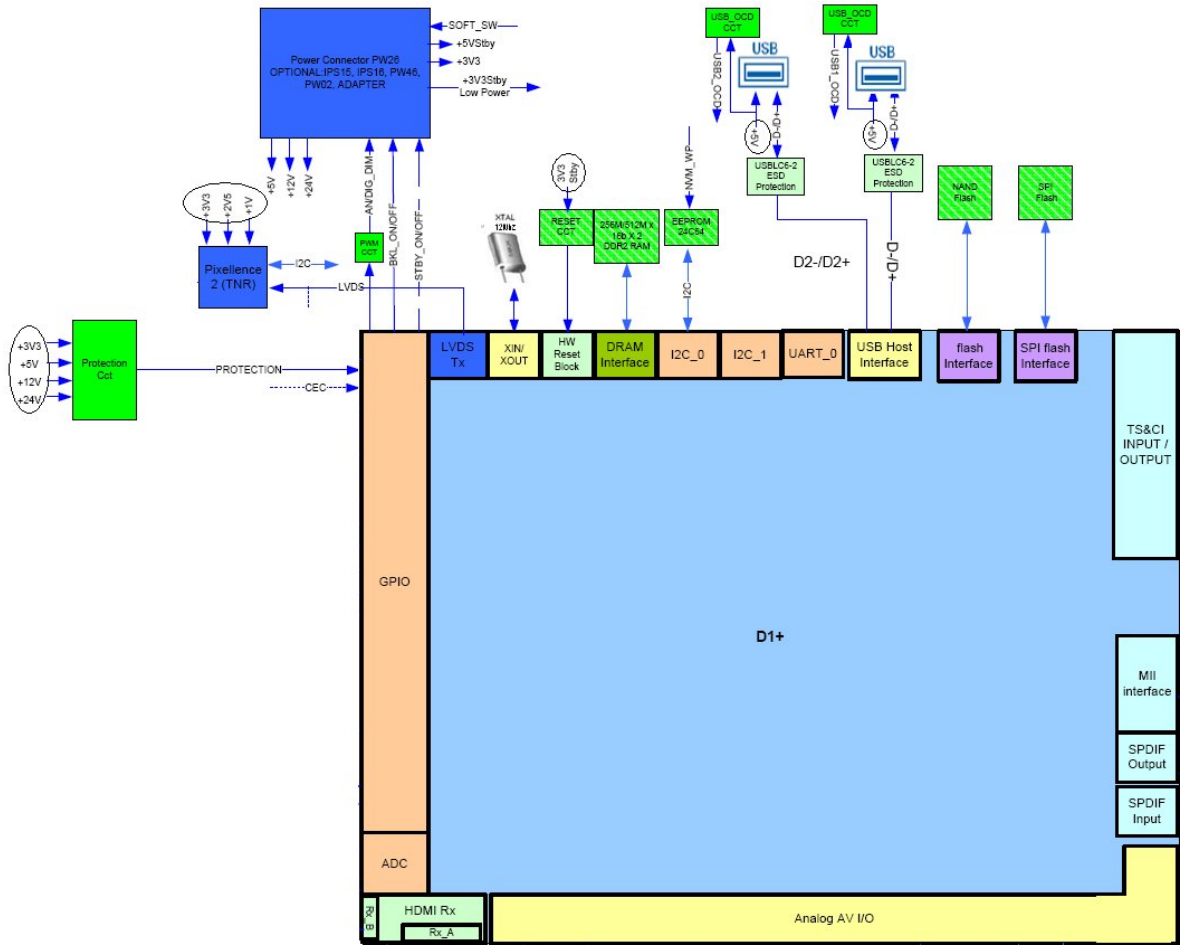
17MB61 General power management block diagram is shown below:

Voltage	Total Current	
3V3	925mA	
3V3 stby	10mA	
5V	2800mA	1500mA PANEL
5V stby	20mA	
1V8	800mA	
1V26	1060mA	
12V	1500mA	PANEL
24V	8250mA	BACKLIGHT

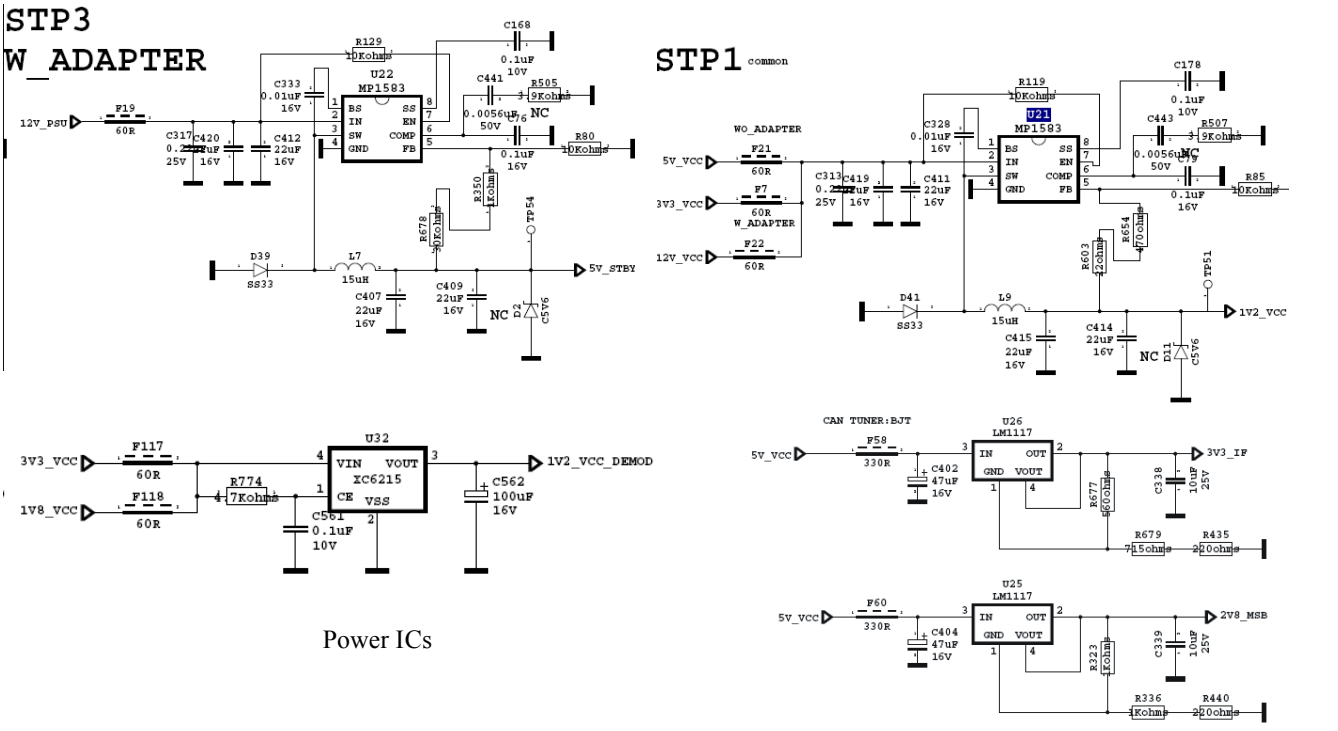
Table 9: Power Consumption

1) These values calculated from max. ratings of existing panels. Meaning values will be lower than calculated values.
2) Total consumption value does not contain the CCFL consumption.





Power Domain



Power ICs

6. MICROCONTROLLER – MSTAR(U157)

MSD9WB7GX-LF-2

GENERAL DESCRIPTION

The MSD9WB7GX-2 is a highly integrated controller IC for LCD/PDP DTV applications with resolutions up to WUXGA (1920x1200). It is configured with an integrated triple-ADC/PLL, a multi-standard TV video and audio decoder, a motion adaptive video de-interlacer, a scaling engine, the MStarACE-3 color engine, an advanced 2D graphics engine, a transport processor, a high-definition (HD) MPEG video decoder, a high-definition (HD) H.264
video decoder, a Real Video decoder, a JPEG video decoder, a MPEG-4 decoder, and a 24-bit DSP for MPEG audio decoding, a DVI/HDCP/HDMI receiver, and a peripheral control unit providing a variety of HDTV control functions.

For digital TV application, the MSD9WB7GX-2 comprises an MPEG-2 transport processor with advanced section filtering capability, an MPEG-2 (MP@HL profile) video decoder, a MPEG-4 decoder, a H.264 video decoder, and an audio DSP decoder for MPEG audio streams, MPEG layer I and II digital audio decoder with analog audio outputs
that are designed to support existing and future DVB-T programs while handling conditional access. Furthermore, it is also possible to decode JPEG, Real Video streams, and MP3 formats from external sources such as USB interface.

For analog TV, the MSD9WB7GX-2 includes NTSC/PAL/SECAM multi-standard video decoder comprising a 3D motion adaptive comb filter and time-based correction, and a NICAM/A2 audio decoder to support worldwide television standards. The MSD9WB7GX-2 is also configured with a VBI processor to decode digital information such as Close Caption/V-chip/teletext/WSS/CGMS-A/VPS. In addition, the MStar advanced LCD TV processor enhances video quality, motion adaptive de-interlacer, picture quality adjustment units, and MStarACE-3 color engine.

With USB 2.0 host controllers, UART, IR, SPI, I2C, and PWM, the MSD9WB7GX-2 fulfills all requirements in advanced DTV sets. Furthermore, MSD9WB7GX-2 can access files from networks with embedded Ethernet MAC and external PHY via the MII/RMII interface. To reduce system costs, the MSD9WB7GX-2 also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

The MSD9WB7GX-LF-2 is composed of several modules:

High performance micro-processor

- Embedded micro-processor supports Linux operating system
- Interrupt controller
- Supports ISP
- Three full duplex UARTs
- DMA engine to speed up large data movement

Transport Stream De-multiplexer

- Two external TS inputs and one internal TS data path
- Supports both parallel and serial TS interface, with or without sync signal
- Maximum TS data rate is 104 Mb/sec for serial or 13 MB/sec for parallel
- 32 general purpose PID filters and section filters for each transport stream de-multiplexer
- One video PES and one audio PES channel
- Supports MHEG5, DVB subtitle and digital teletext
- Supports additional audio/video/PCR filters
- Supports TS DMA channel for time-shift
- Supports AES encryption/decryption

MPEG-2 A/V Decoder

- ISO/IEC 13818-2 MPEG-2 video MP@HL
- Automatic frame rate conversion
- Supports resolution in HDTV (1080i, 720p) and SDTV
- Supports MPEG-1, MPEG-2 (Layer I/II), Dolby1 Digital (AC-3), and AAC audio decoding
- Supports Dolby Digital Plus (E-AC-3)2 decoding, and Dolby Digital Compatible Output (DDCO) for HE-AAC to DD transcodingOpt i ona l

MPEG-4 Video Decoder

- ISO/IEC 14496-2 MPEG-4 ASP video decoding
- Supports resolution in HDTV (1080p@30fps)
- Supports DivX3 Home Theater or HD profileOpt i ona l

H.264 Decoder

- ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.0) video decoding
- Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
- Supports resolution up to 1080p@30fps
- Supports CABAC and CAVLC stream types
- Processing of ES and PES streams, extractions and provision of time stamps

RealMedia DecoderOpt i ona l

- Supports maximum resolution up to 720p@30fps
- Supports RV8, RV9, RV10, RA8-LBR and HE-AAC decoders
- Supports file formats with RM and RMVB
- Supports Picture Re-sampling
- Supports in-loop de-block for B-frame

Hardware JPEG

- Supports sequential mode, single scan
- Supports both color and grayscale picture
- Operates in scan unit; hardware decoder will handle the bit stream after scan header
- Supports programmable region of interest (ROI)
- Supports format: 422/411/420/444/422T
- Decoded picture will be stored in DRAM with UYVY format
- Supports scaling down ratio: 1/2, 1/4, 1/8, applied to height and width simultaneously
- Supports picture rotation

NTSC/PAL/SECAM Video Decoder

- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM
- Automatic TV standard detection
- Motion adaptive 3D comb filter for NTSC/PAL
- Eight configurable CVBS & Y/C S-video inputs
- Supports Teletext level-1.5, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE
- Two CVBS video outputs

Multi-Standard TV Sound Processor

- Supports BTSC/A2/EIA-J demodulation in NTSC and A2/NICAM/FM/AM demodulation in PAL
- Supports MTS Mode Mono/Stereo/SAP in BTSC/ EIA-J and Mono/Stereo/Dual in A2/NICAM
- L/R audio line-in x6 and SIF audio input
- L/R speaker and 2 additional L/R audio line-out
- Built-in audio sampling rate conversion (SRC)
- Built-in audio ADC
- Built-in audio DAC's
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround, and treble/bass
- Advanced soundOpti o na l available (Dolby, SRS1 , BBE2... etc)
- Supports digital audio format decoding:
  - MPEG-1, MPEG-2 (Layer MI), MP3, AC-3 (Dolby Digital), AAC-LC, WMA
  - E-AC-3 (Dolby Digital Plus) decoding and E-AC-3 to AC-3 conversion at the same time

Digital Audio Interface

- I2S digital audio input & output
- S/PDIF digital audio input & output
- HDMI audio channel processing capability
- Programmable delay for audio/video synchronization

Analog RGB Compliant Input Ports

- Three analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

Auto-Configuration/Auto-Detection

- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Port

- Three DVI/HDCP/HDMI input ports support up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
- High Definition Multimedia Interface (HDMI) 1.3 compliant receiver with CEC (Consumer Electronics Control) support
- Long-cable tolerant robust receiving

High-Performance Scaling Engines

- Fully programmable shrink/zoom capabilities
- Nonlinear video scaling supports various modes including Panorama

Video Processing & Conversion

- 3D motion adaptive video de-interlacers with edge-oriented adaptive algorithm for smooth low-angle edges
- Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
- MStar 3rd Generation Advanced Color Engine (MStarACE-3) automatic picture enhancement:
  - Brilliant and fresh color
  - Blue Stretch
  - Intensified contrast and details
  - Vivid skin tone
  - Sharp edge
  - Enhanced depth of field perception
  - Accurate and independent color control
- Supports sRGB and xvYCC color processing
- Supports HDMI 1.3 deep color format
- Supports enhanced and seamless color mapping for wider gamut panels
- 10-bit internal data processing
- Programmable 12-bit RGB gamma CLUT
- 3D video noise reduction
- MPEG artifact removal including de-blocking and mosquito noise reduction
- Frame rate conversion

Output Interface

- Supports up to 10-bit dual LVDS WUXGA (1920x1200) panel interface
- Supports 2 data output formats: Thine & TI data mappings
- Compatible with TIA/EIA
- With 6/8 bits optional dithered output
- Spread spectrum output frequency for EMI suppression

CVBS Video Output

- Supports CVBS bypass output
- Built-in video encoder for encoding digital video into CVBS output

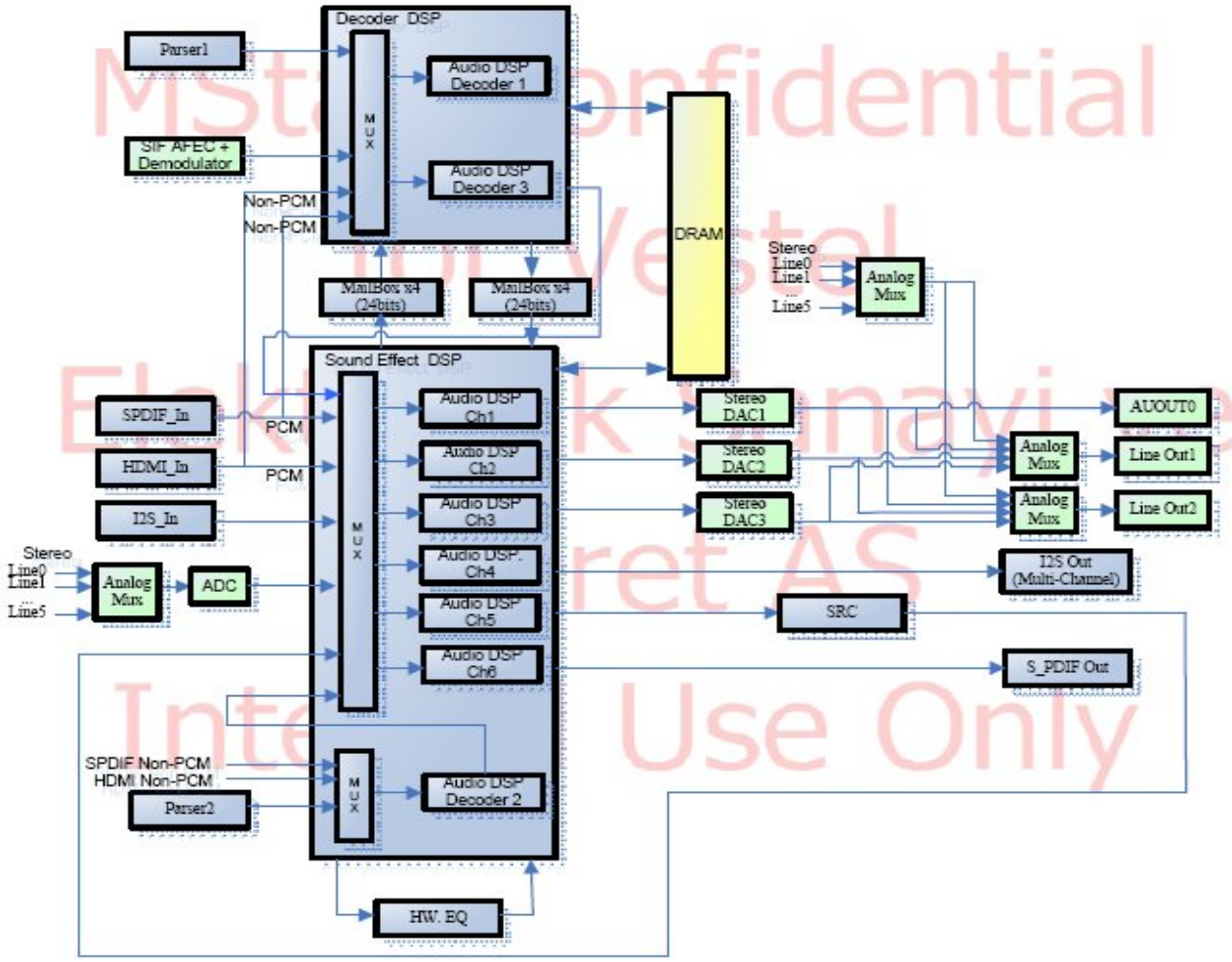
2D Graphics Engine

- Point draw, line draw, rectangle draw/fill and text draw
- BitBlt and stretch BitBlt
- Raster Operation (ROP)

Miscellaneous

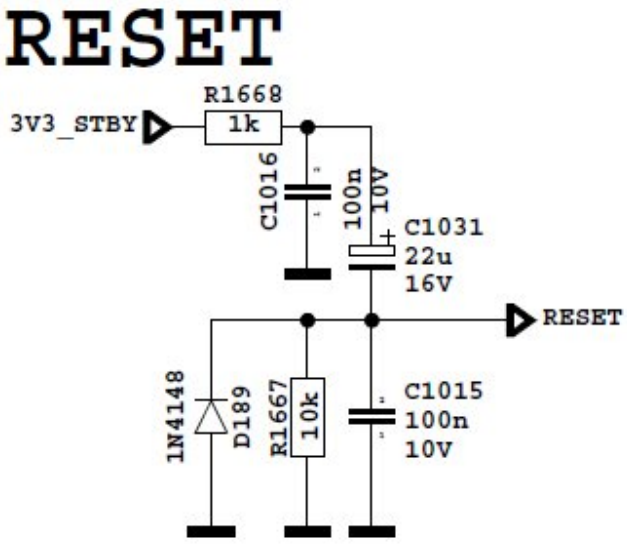
- DRAM controller to support up to two 16-bit DDR2 interfaces
- Supports Common Interface for conditional access
- SPI serial interface for external SPI flash
- Parallel interface for external parallel NOR flash and NAND flash
- Build-in 10/100Mbps Ethernet Mac
- High efficiency power control module
- Two ports of USB 2.0 host controller with the flexibility for connecting external storage devices
- 505-ball TFBGA package
- Operating at 1.26V (core), 1.9V (DDR2), and 3.3V (I/O and analog)

6.1. MSTAR Block Diagram



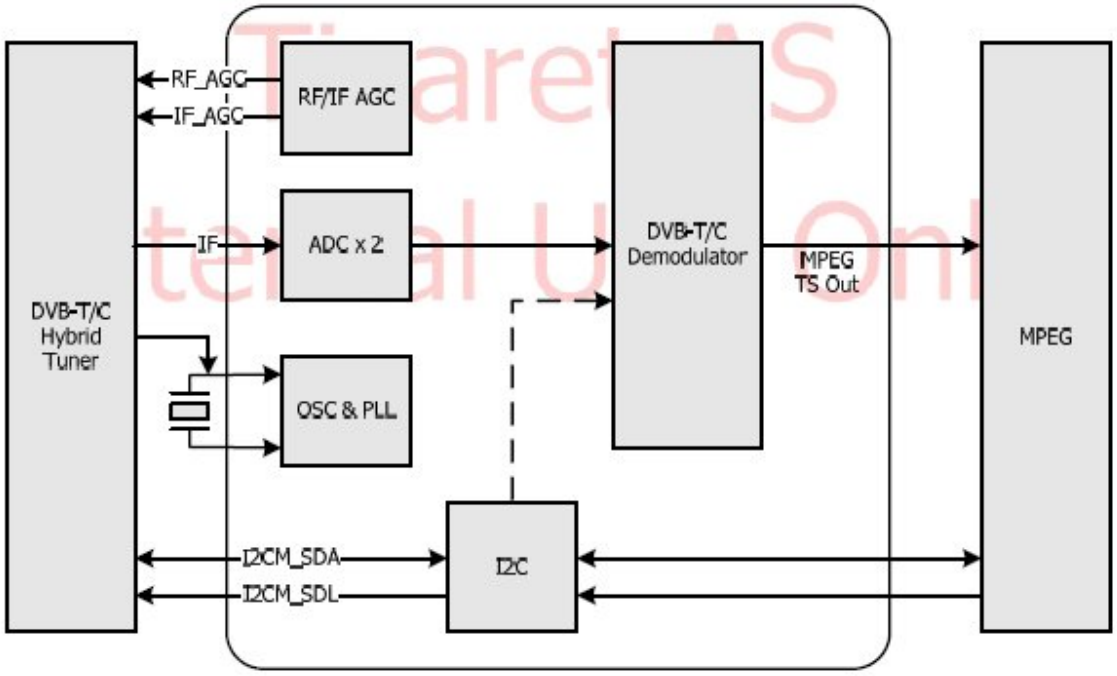
6.2. Reset Circuit

Reset circuit using for initiliazing main Mstar IC. Reset condition is high and nomal working condition is low for RESET pin.



7. CI INTERFACE

7.1 Block Diagram



7.1 CI Interface Power Switch

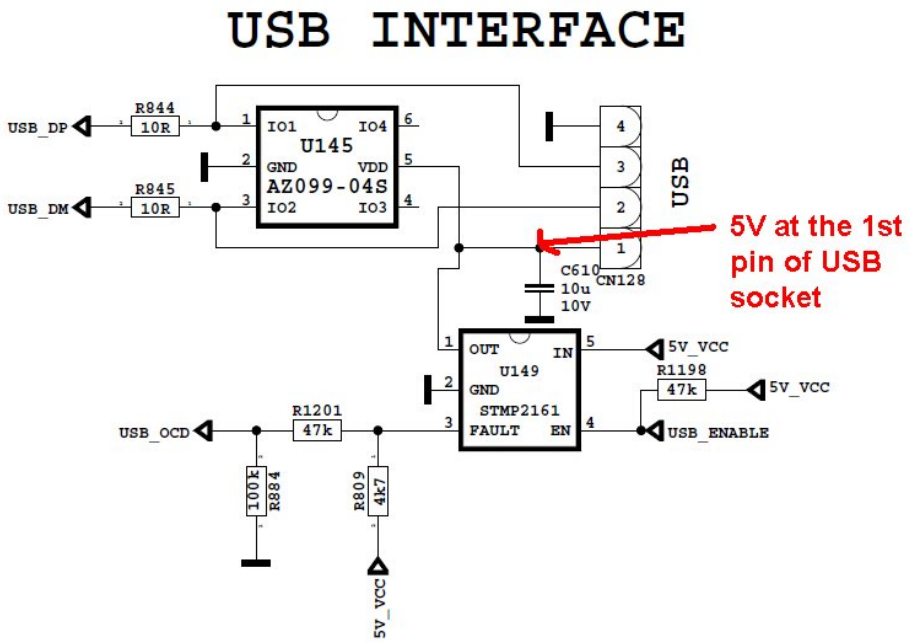
It is used for CI module supply, when Module is inserted (it means CI detect is low) This circuit is opened or closed by CI_POWER_CTRL port of main uController

8. USB INTERFACE

Main Concept IC has integrated 2 USB 2.0 interface. One of them is used for ethernet function, the other one is used for USB connectivity for last user. Last user can play video, picture and audio files. Also digital channels can be record to externall storage device by this interface. All SW files can be updated with interface.

USB circuit has 3 main parts

- Integrated USB 2.0 Host interface of D3 (U157)
- Protection IC (U145)
- Over Curent Protection IC (U149)



9. DDR2 SDRAM 8M × 4 BANKS × 16 BIT (W9751G6JB) (U154, U155)

9.1. General Description

The W9751G6JB is a 512M bits DDR2 SDRAM, organized as 8,388,608 words × 4 banks × 16 bits. This device achieves high speed transfer rates up to 1066Mb/sec/pin (DDR2-1066) for general applications. W9751G6JB is sorted into the following speed grades: -18, -25 and -3. The -18 is compliant to the DDR2-1066/CL7 specification. The -25 is compliant to the DDR2-800 (5-5-5) or DDR2-800 (6-6-6) specification. The -3 is compliant

to the DDR2-667 (5-5-5) specification. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CLK rising and CLK falling). All I/Os are synchronized with a single ended DQS or differential DQS- DQS pair in a source synchronous fashion.

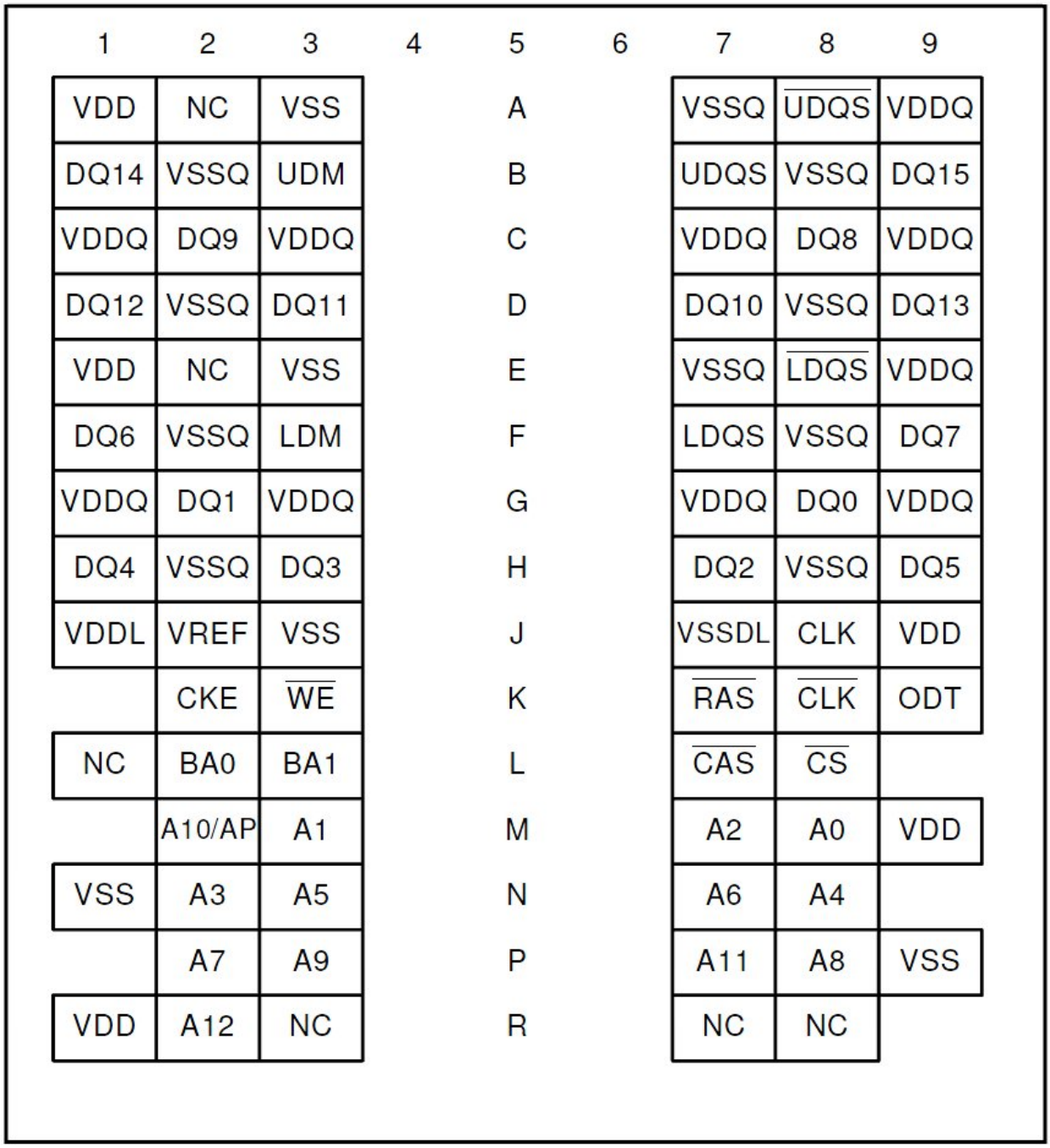
9.2. Features

- Power Supply: VDD, VDDQ = 1.8 V± 0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3, 4, 5, 6 and 7
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DQS andDQS) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLK)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Posted CAS programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

9.3. Electrical Characteristics

SYM.	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	2, 3
VTT	Termination Voltage (System)	VREF - 0.04	VREF	VREF + 0.04	V	4

9.4. Pinning



1	2	3	4	5	6	7	8	9
VDD	NC	VSS		A		VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM		B		UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ		C		VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11		D		DQ10	VSSQ	DQ13
VDD	NC	VSS		E		VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM		F		LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ		G		VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3		H		DQ2	VSSQ	DQ5
VDDL	VREF	VSS		J		VSSDL	CLK	VDD
	CKE	$\overline{\text{WE}}$		K		$\overline{\text{RAS}}$	$\overline{\text{CLK}}$	ODT
NC	BA0	BA1		L		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1		M		A2	A0	VDD
VSS	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	VSS
VDD	A12	NC		R		NC	NC	

BALL NUMBER	SYMBOL	FUNCTION	DESCRIPTION
M8,M3,M7,N2,N8,N3,N7,P2,P8,P3,M2,P7,R2	A0–A12	Address	Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0–A12. Column address: A0–A9. (A10 is used for Auto-precharge)
L2,L3	BA0–BA1	Bank Select	BA0–BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
G8,G2,H7,H3,H1,H9,F1,F9,C8,C2,D7,D3,D1,D9,B1,B9	DQ0–DQ15	Data Input / Output	Bi-directional data bus.
K9	ODT	On Die Termination Control	ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
F7,E8	LDQS, $\overline{\text{LDQS}}$	LOW Data Strobe	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS corresponds to the data on DQ0–DQ7. $\overline{\text{LDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
B7,A8	UDQS, $\overline{\text{UDQS}}$	UP Data Strobe	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS corresponds to the data on DQ8–DQ15. $\overline{\text{UDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
L8	$\overline{\text{CS}}$	Chip Select	All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple ranks. $\overline{\text{CS}}$ is considered part of the command code.
K7,L7,K3	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Command Inputs	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
B3,F3	UDM LDM	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
J8,K8	CLK, $\overline{\text{CLK}}$	Differential Clock Inputs	CLK and $\overline{\text{CLK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{\text{CLK}}$. Output (read) data is referenced to the crossings of CLK and $\overline{\text{CLK}}$ (both directions of crossing).
K2	CKE	Clock Enable	CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
J2	V_{REF}	Reference Voltage	V_{REF} is reference voltage for inputs.
A1,E1,J9,M9,R1	V_{DD}	Power Supply	Power Supply: 1.8V ± 0.1V.
A3,E3,J3,N1,P9	V_{SS}	Ground	Ground.
A9,C1,C3,C7,C9,E9,G1,G3,G7,G9	V_{DDQ}	DQ Power Supply	DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2,D8,E7,F2,F8,H2,H8	V_{SSQ}	DQ Ground	DQ Ground. Isolated on the device for improved noise immunity.
A2,E2,L1,R3,R7,R8	NC	No Connection	No connection.
J7	V_{SSDL}	DLL Ground	DLL Ground.
J1	V_{DDL}	DLL Power Supply	DLL Power Supply: 1.8V ± 0.1V.

Headphone Amplifier-TDA1308

The TDA1308 is an integrated class AB stereo headphone driver.

- Power supply maximum 60 mW to 32Ω (THD<0.1%)
- 5V single supply
- SNR 110 dB
- Power supply ripple rejection

- Typically 3 mA supply current at no load
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance

high signal-to-noise ratio
high slew rate
low distortion
· Large output voltage swing.

Pin configuration and description is given in Figure 16 and Table 18.

SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
V_{DD}	8	positive supply

Table 18: Pin configuration

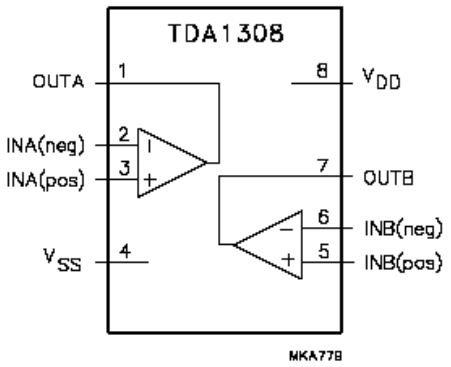


Figure 19: Pin configuration

INB (pos) and INA (pos) are connected to a reference voltage 2.5 V by dividing VDD supply. INA (neg) and INB (neg) is connected to HEADPHONER, HEADPHONEL outputs of VCTH. Those audio outputs are parallel to LINE_OUT connectors. Headphone has also detection property from the connector. It is controlled by VCTH GPIO pin “HP Detect”.

Demodulators

MSB1210

The MSB1210 is the world’s 1st hybrid demodulator to receive both analog terrestrial TV and digital TV signals. It contains the state of the art Signal Processing to offer high quality receptionof analog terrestrial TV signals compliant with PAL B(G, PAL I standards. It also contains a superior COFDM demodulator. It can be used in all 2K, 4K and 8K modes with 5,6,7 and 8 MHz channels and is capable of receiving all modes of transmission.

The device includes a high performance 11 bit A/D converter capable of accepting direct IF at 36 or 44 MHz. It can also support low IF and ZIF signaling. Sampling rates required for all these frequencies in OFDM channels can be generated from a single 24MHz crystal.

The device demodulates standard- and high-definition television signals according to European digital television broadcast standards (terrestrial TV). Analog TV broadcasts are translated to baseband video and digital audio output signals.

Features

- Integrated DVB-T Receiver
  - Compliant with DVBT(ETSI ET 300 744)
  - Nordig-Unified, D-Book, E-Book IEC62002 compliant
  - Supports single or dual AGC control
  - CCI and ACI rejection capability
- Integrated VIF Receiver
  - Multistandart analog TV receiver applications
  - Digital low IF architecture
  - Maximum IF gain of 48dB

- Support for legacy analog standards:
  - ATV PAL/SECAM/NTSC VIF demodulator
  - ATV PAL/SECAM/NTSC (FM/A2, AM, BTSC,SAP, EIA-J, NICAM) audio demodulator/decoder
  - FM Radio with RDS / RBDS

- Comfortable software drivers for integration of tuner and demodulator

- Interfaces:
  - IF and (optional) RF gain control outputs to tuners and sense input for tuner output signal
  - Parallel and serial MPEG_TS outputs
  - Analog CVBS and SIF output
  - I2S digital audio output (8-49 kHz with 16/32 bit per sample) for analog TV audio
  - I2C master/slave interface
  - Secondary I2C interface for tuner control
  - JTAG
  - GPIO

- Frontend integration and flexibility:
  - AGC controls: RF-AGC, IF-AGC
  - Support for low- / near-zero-IF

Block Diagram

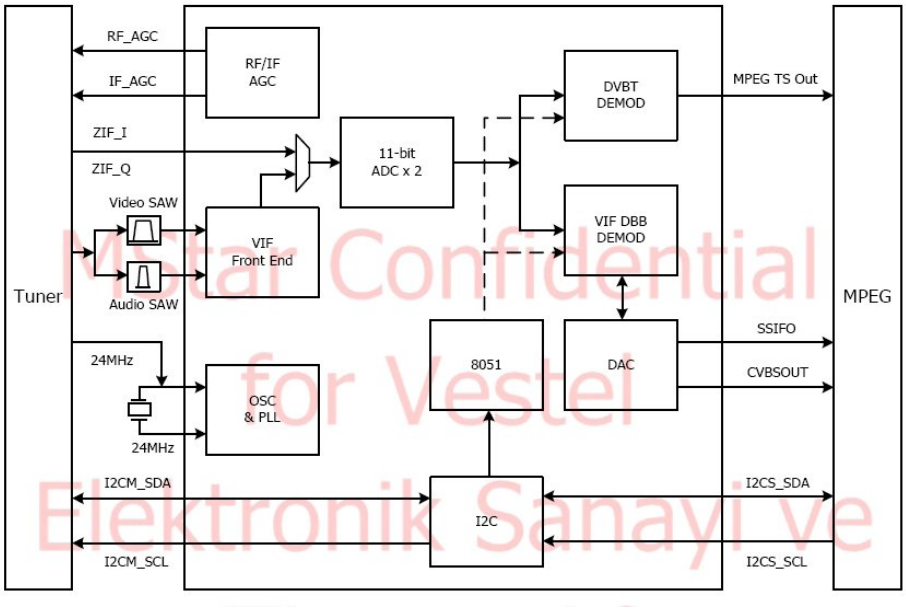


Figure 20: MSB1210 Block Diagram

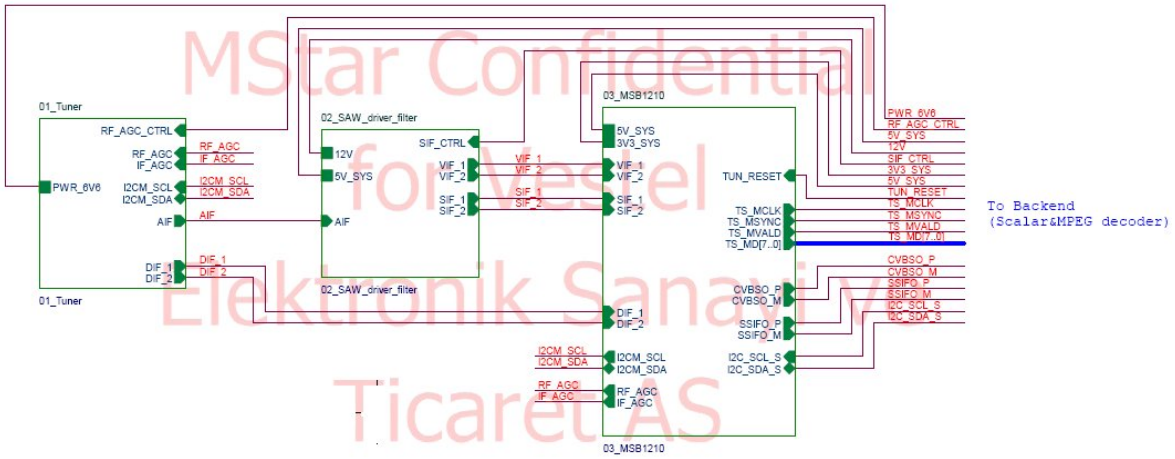


Figure 21: MSB1210 Application Circuit

MSB1222

The MSB1222 contains a superior COFDM demodulator that is Nordig Unified 1.0.3/2.0, D-Book5.0, E-Book, DVB-T compliant. It can be used in all 2K, 4K and 8K modes with 5, 6, 7 and 8 MHz channels and is capable of receiving all modes of transmission.

The MSB122 also includes a QAM demodulator which supports 16, 32, 64, 128 and 256 QAM while being compliant to DVB-C, ITU_T J.83 Annex A/C and China GY/T 170-2001.

The device includes low-power, high performance A/D converters capable of accepting direct IF at 36/44 MHz. Furthermore, it supports low IF and ZIF signaling.

Features

- DVB-T Demodulator
  - Compliant with DVB-T
  - All digital demodulation and timing recovery loops
  - CCI and ACI rejection capability
  - Impulse-Noise suppression
  - Direct 36MHz, 44MHz IF sampling scheme from tuner
- DVB-C Demodulator
  - Compliant with DVB-C(EN300429) and ITU-T J.83 Annex A/C
  - Supports symbol rates up to 7M Baud
  - Single IF filter bandwidth for all symbol rates
- Configurable parallel/serial MPEG2 transport stream interface
- Supports I2C interface

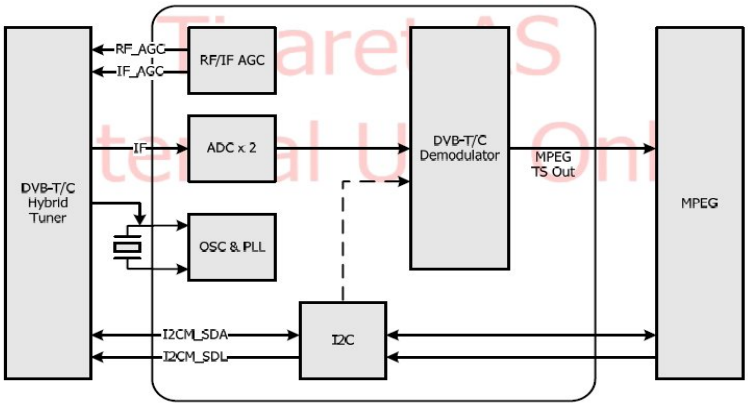


Figure 22: MSB1222 Block Diagram

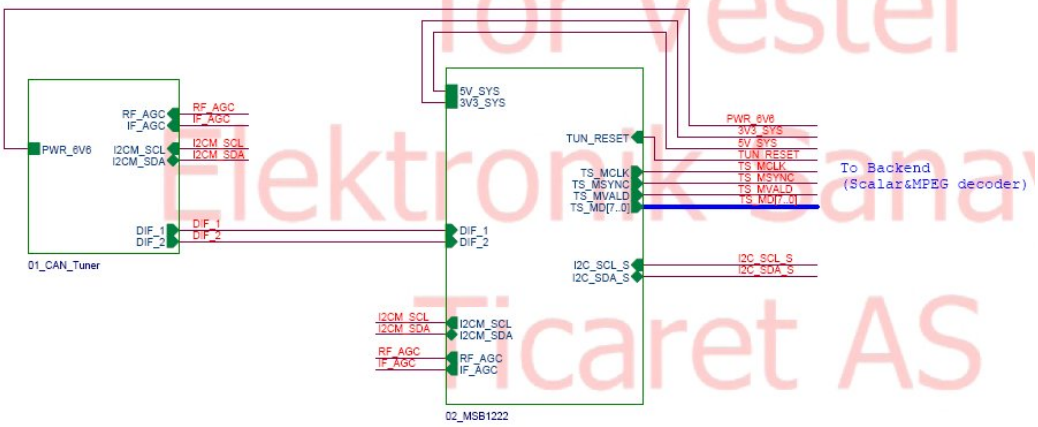


Figure 23: MSB1222 Application Circuit

CXD2820D

The Sony CXD2820R is a combined DVB-T2, DVB-T and DVB-C demodulator that conforms to the ETSI EN 302-755 (second generation Terrestrial) ETSI EN 300-744 (Terrestrial) and ETSI EN 300-429 (Cable) standards.

The CXD2820R is a DVB-T2 demodulator offering class-leading performance, optimised BOM requiring no external memory and low processor overhead. It includes a

highly integrated dual-core DVB-T and DVB-C demodulator which complies with all relevant European performance standards.

Features

- Supports all DVB-T2 modes, including
    - Single and multiple-PLPs
    - SISO and MISO transmission
- Simple API
    - Fully-automatic acquisition
    - Fully-automatic L1-signalling decoding
    - Automatic guard-interval detection
    - Automatically-calculated constant-rate TS output (using L1signalling and ISSY)
- Acquisition range ±857kHz
- Stream processor for automatic common- and data-PLP combination
- Null-packet insertion
- Access to channel echo profile and constellation via I2C
- Single, 41MHz crystal (can be shared with CXD2813R analogue demod IC)
- High performance differential signal ADC
- RF power level monitor ADC
- Low IF and high IF (36MHz) mode input
- Fast 400kHz I2C compatible bus interface
- Quiet I2C interface for dedicated tuner control
- Automatic IF AGC and optional programmable RF AGC/GPIO functions
- Configurable parallel and serial MPEG-2 TS outputs with smoothing buffer
- 3.3V, 2.5V, 1.2V supplies
- Temperature range -20°C to +85°C • 64 pin exposed-pad LQFP 10mm x 10mm package
- RF power level monitor ADC
- 64 pin exposed-pad LQFP 10mm x 10mm package

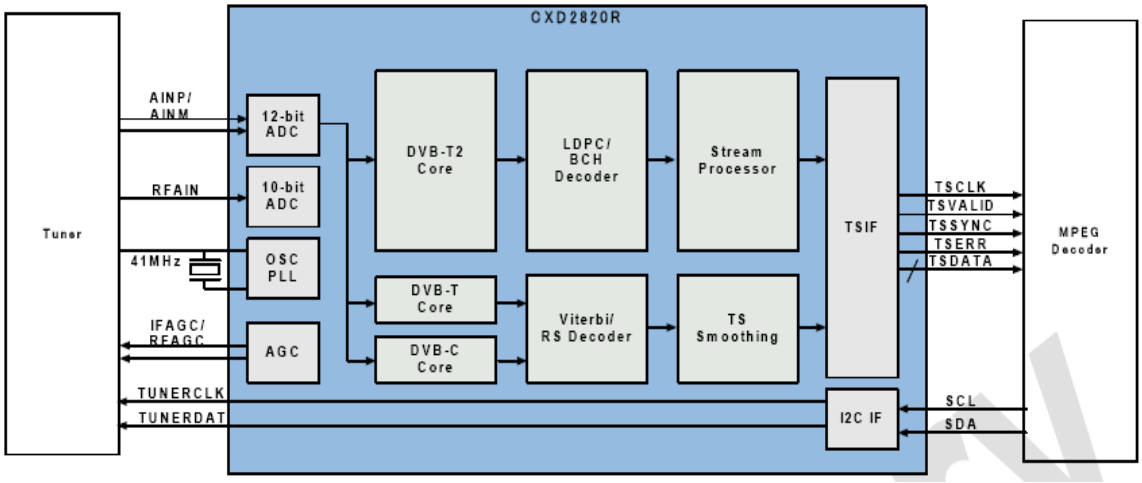
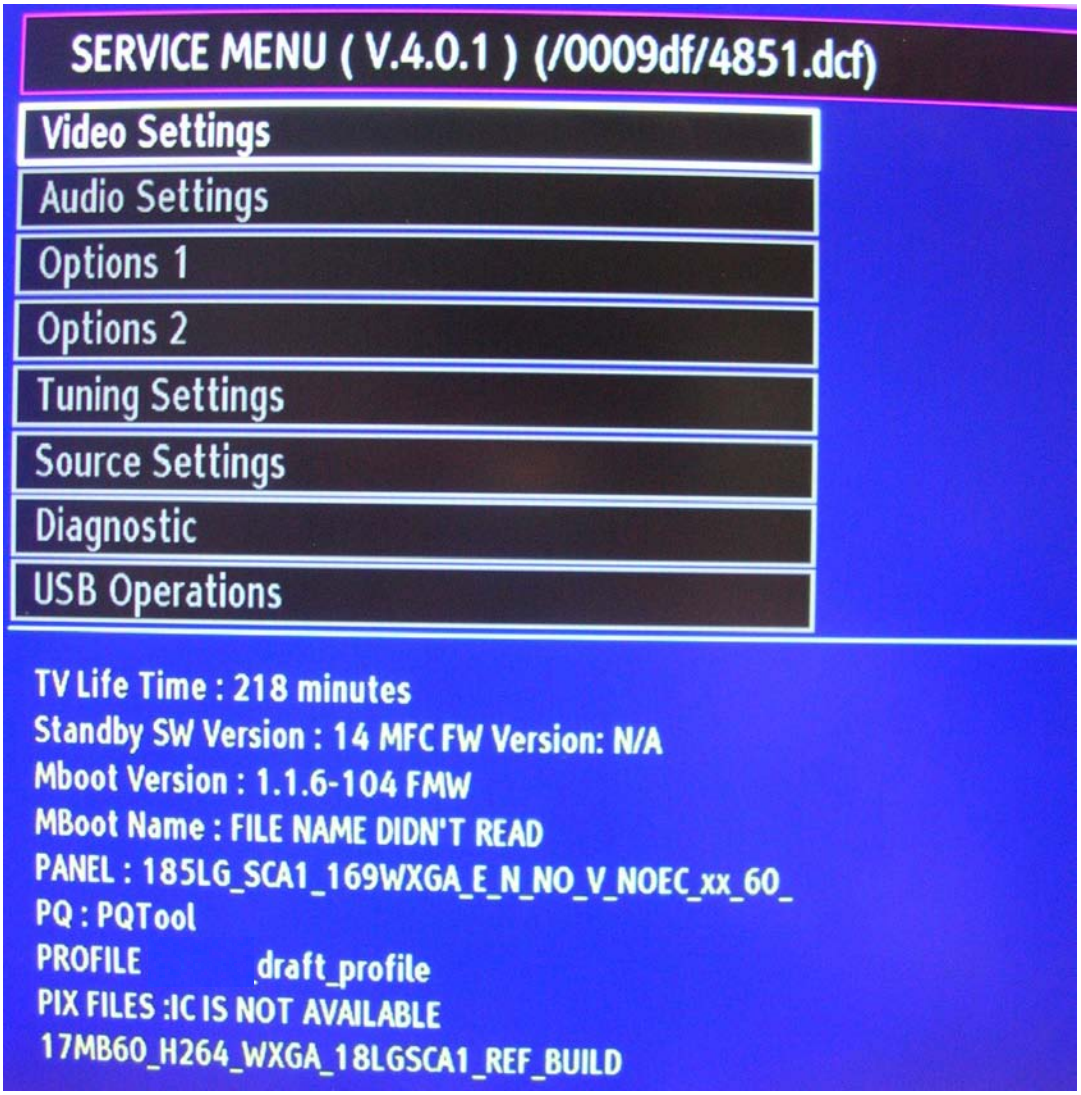


Figure 24: CXD2820D Block Diagram

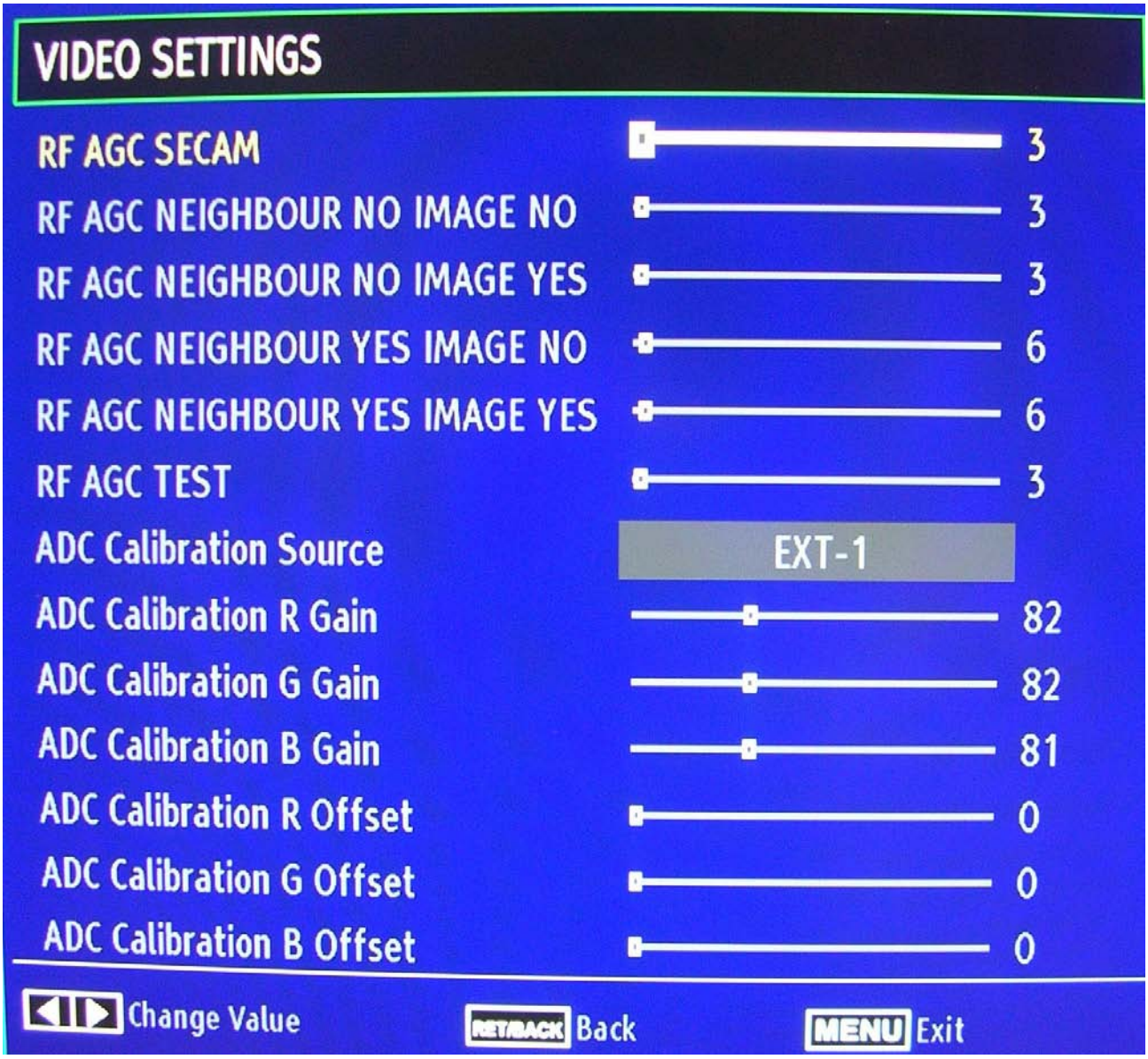
10. SERVICE MENU SETTINGS

In order to reach service menu, First Press **"MENU"** Then press the remote control code two times, which is **"4725"**.

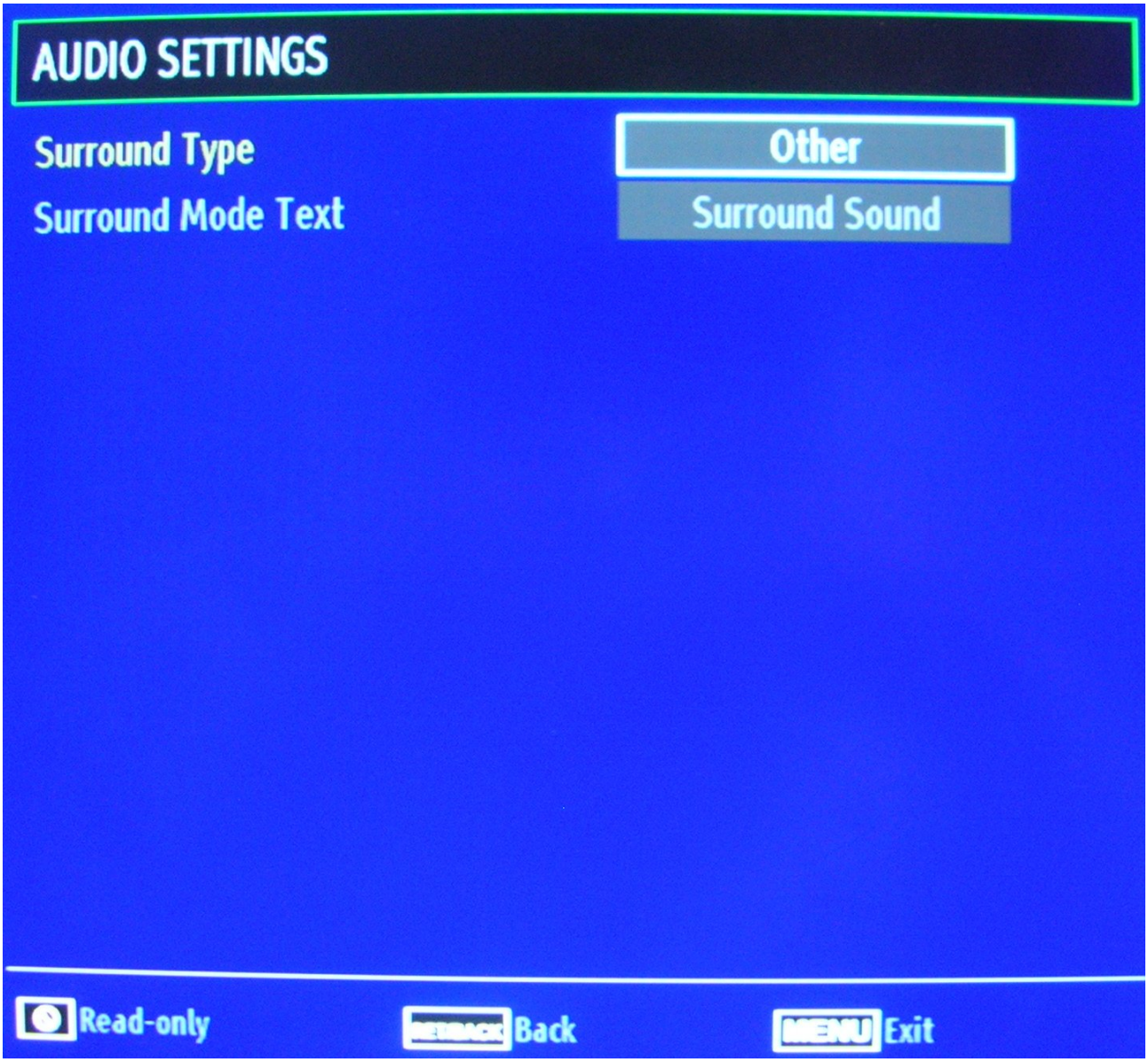
In first screen following items can be seen:



10.1. Video Settings

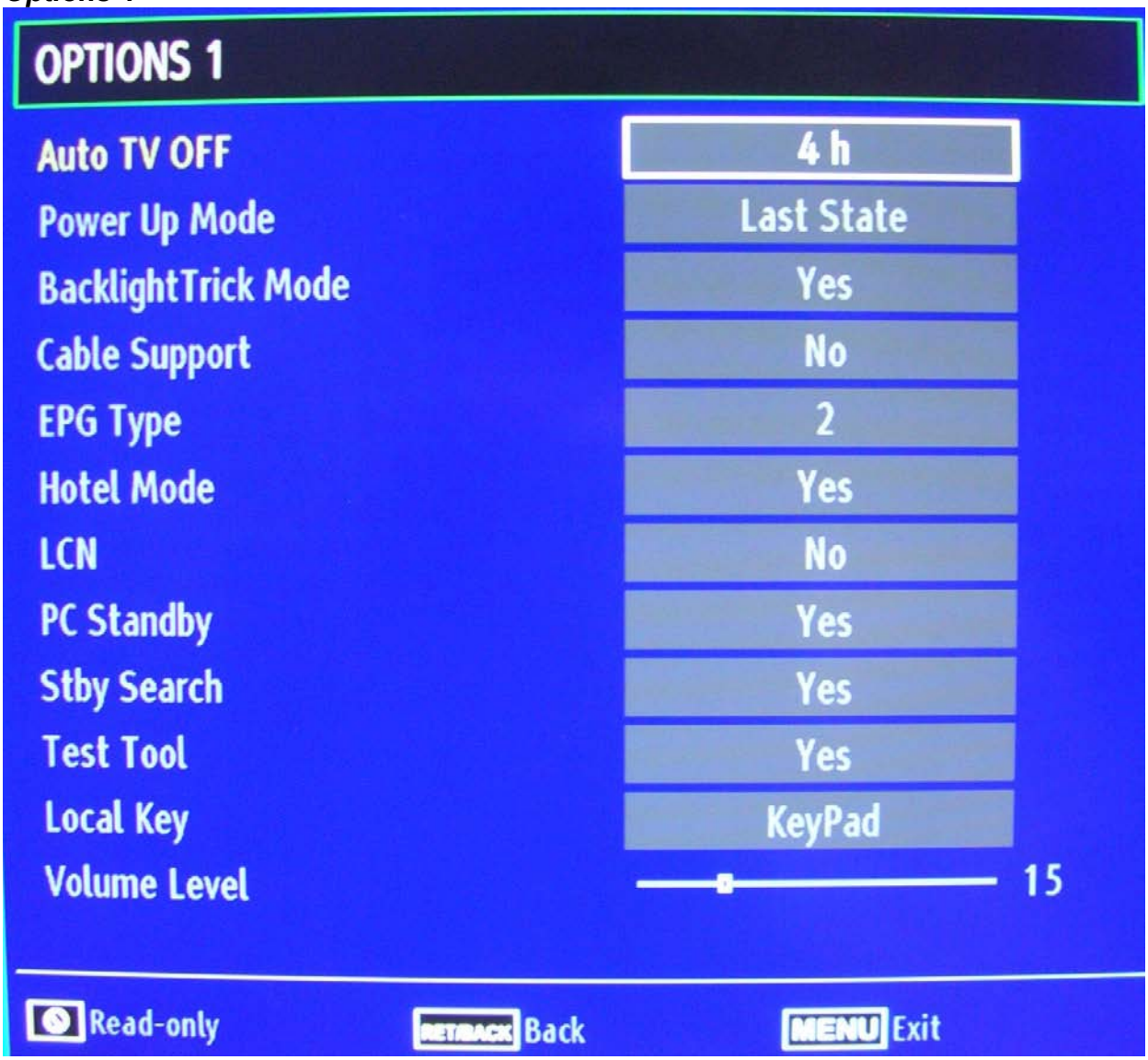


10.2. Audio Settings

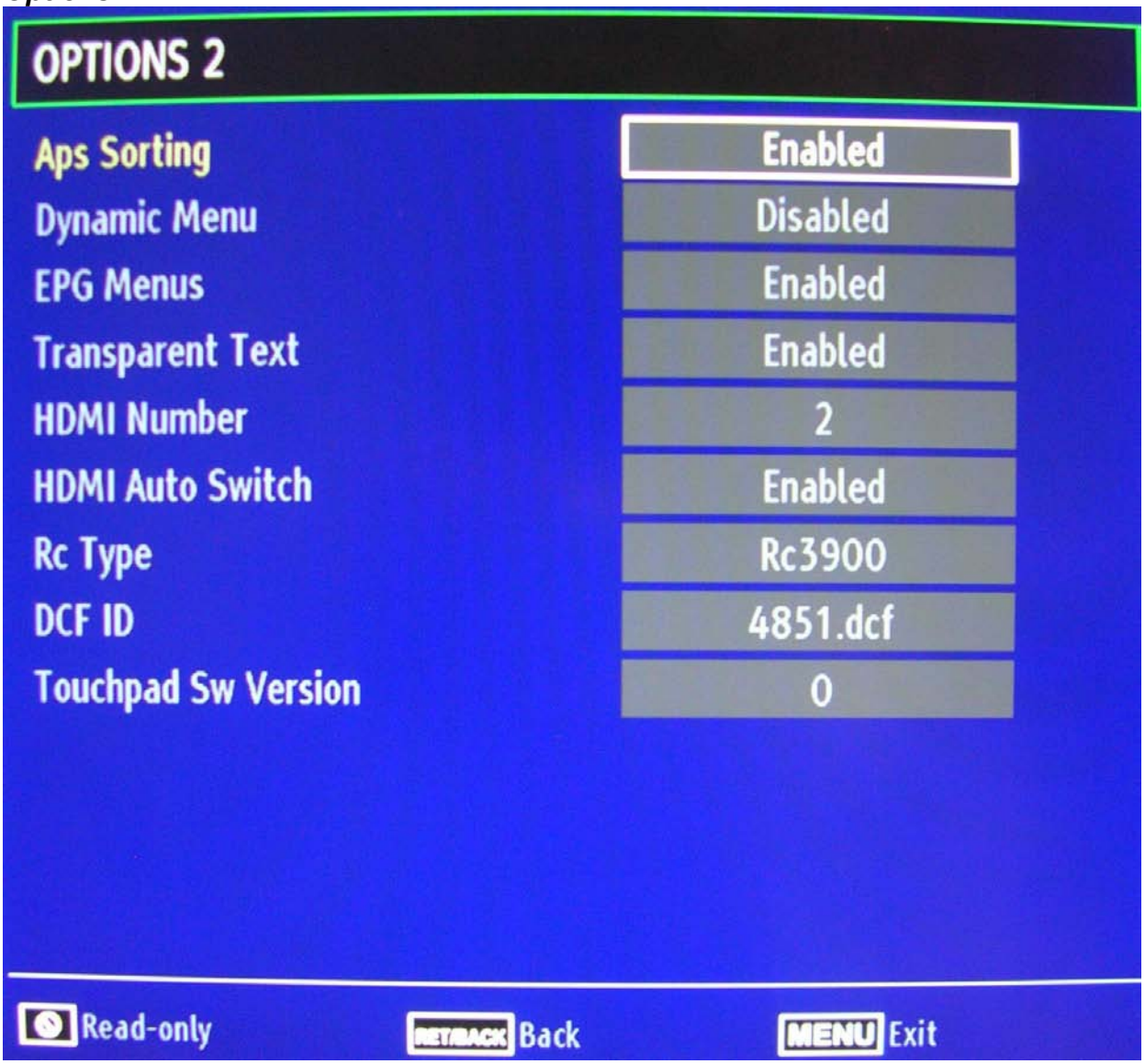


10.3. Options

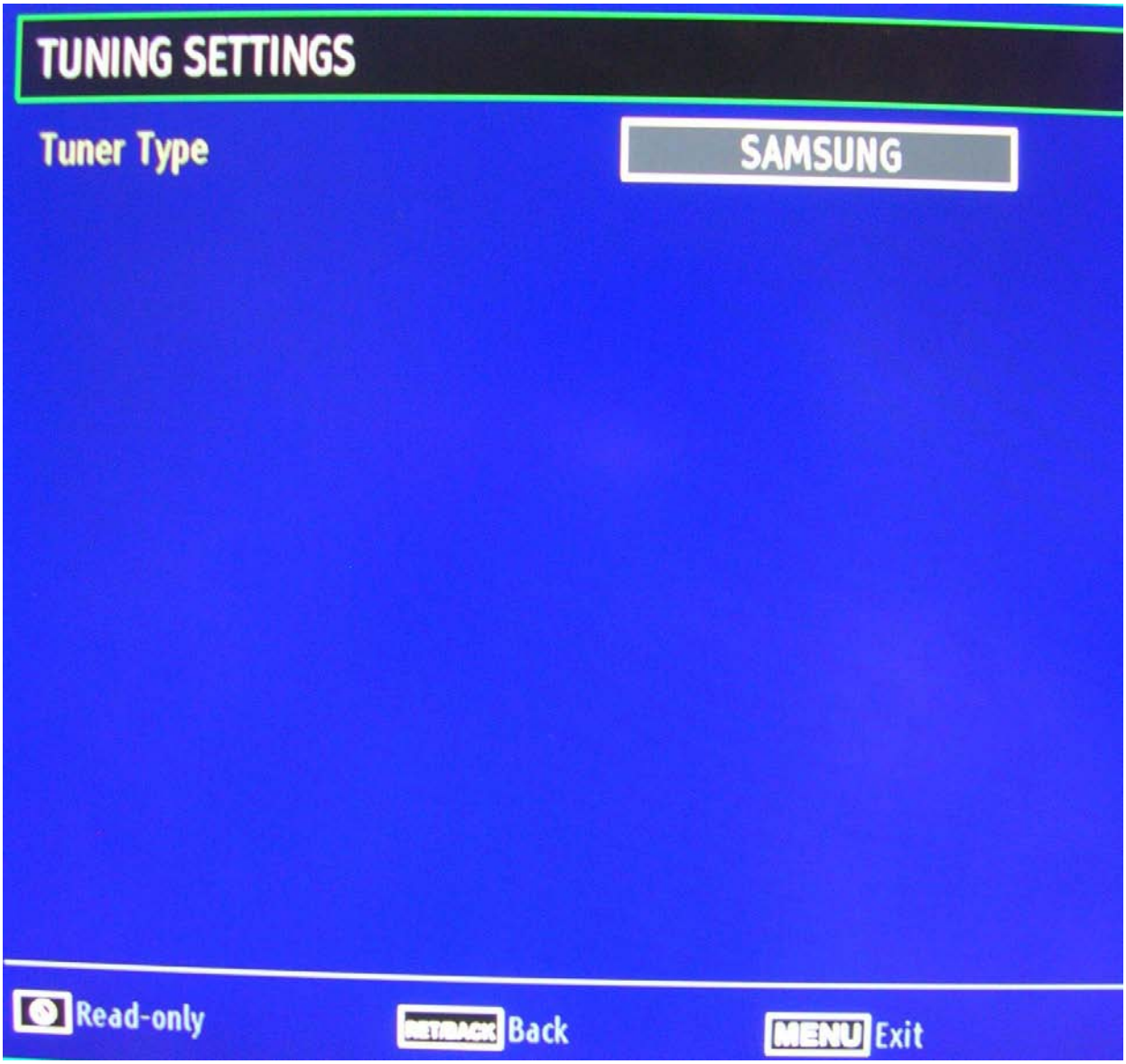
Options-1



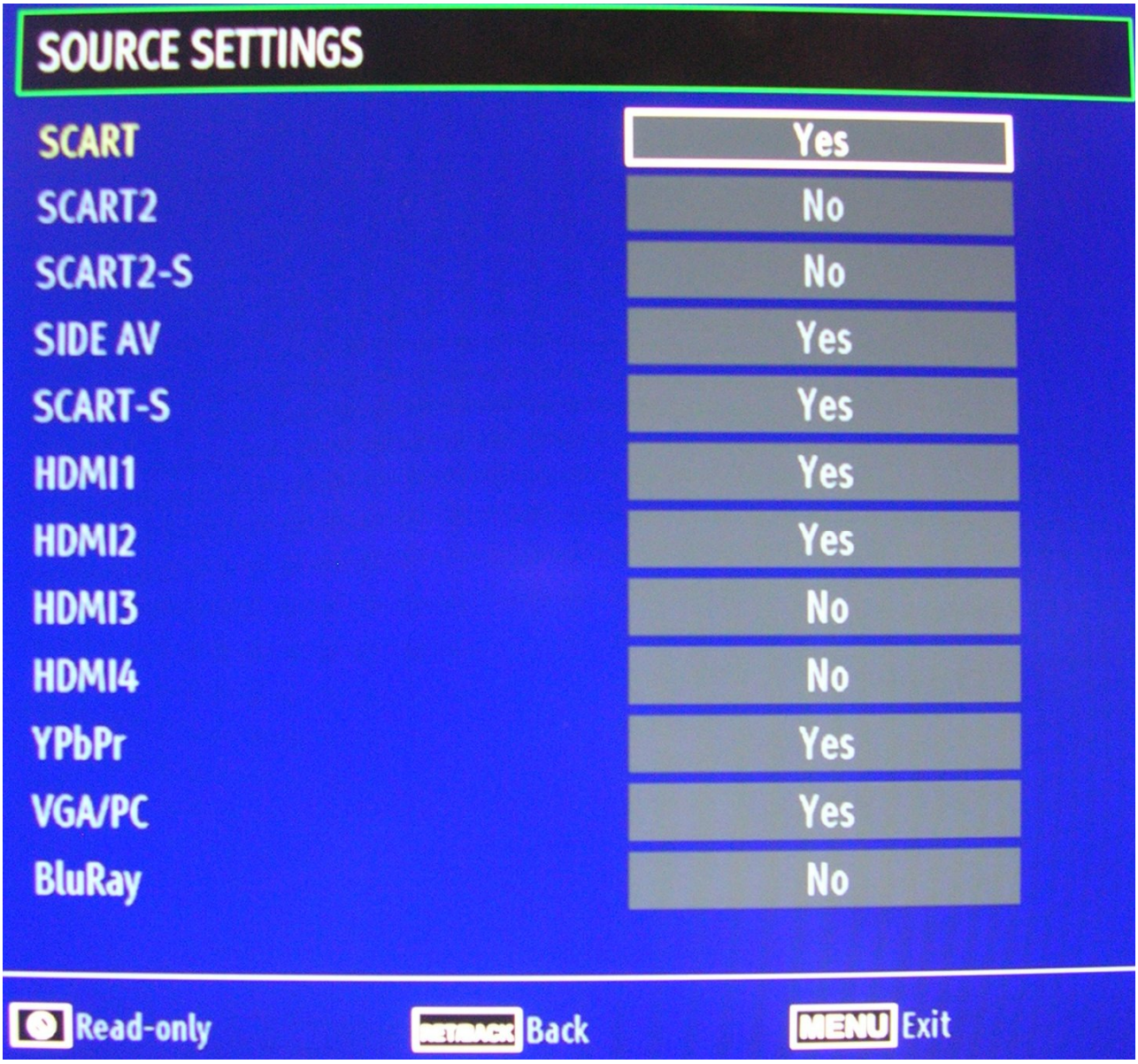
Options-2


OPTIONS 2
Aps Sorting
Enabled
Dynamic Menu
Disabled
EPG Menus
Enabled
Transparent Text
Enabled
HDMI Number
2
HDMI Auto Switch
Enabled
Rc Type
Rc3900
DCF ID
4851.dcf
Touchpad Sw Version
0
Read-only
RETURN/BACK Back
MENU Exit

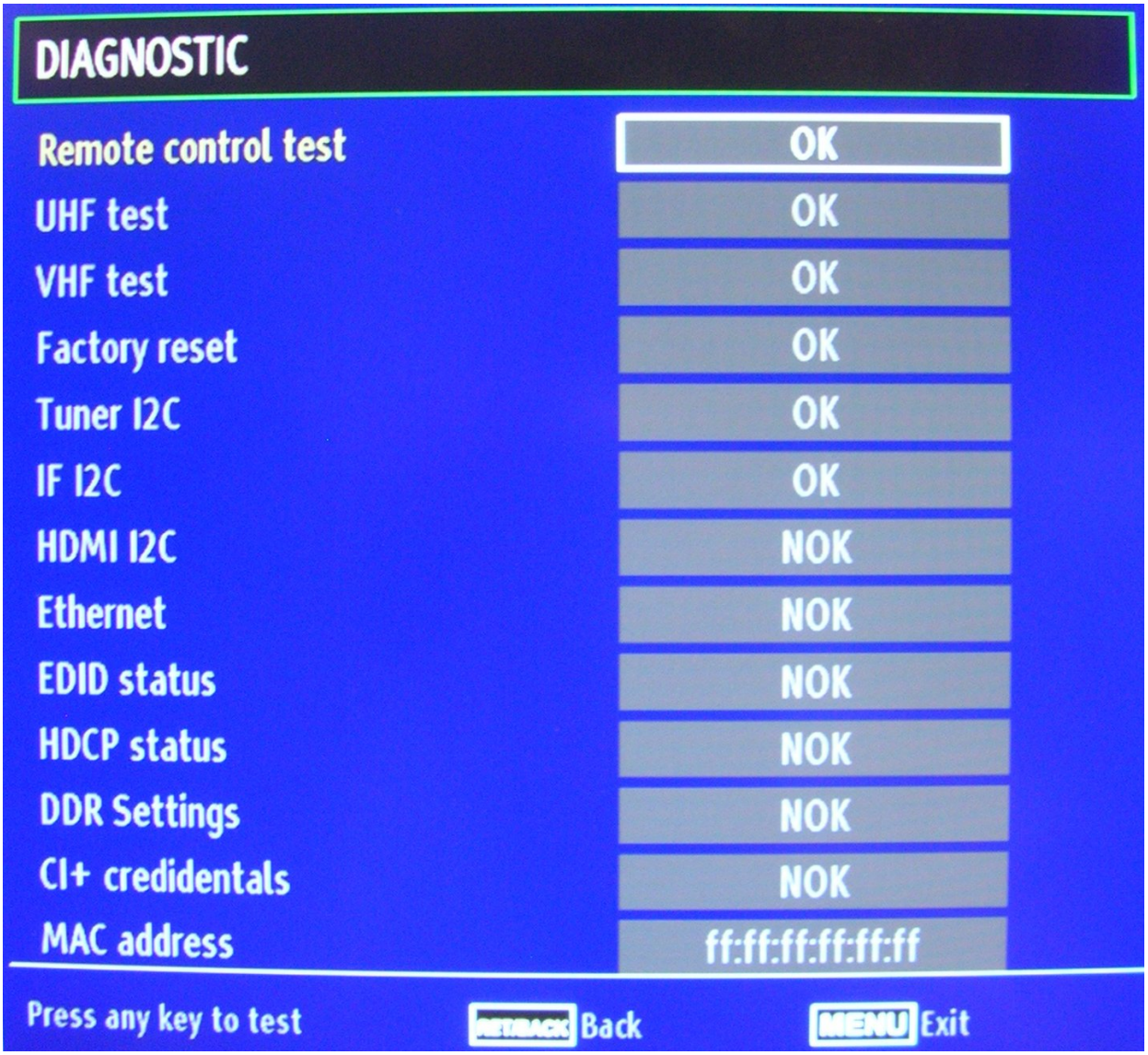
10.4. Tuning Settings



10.5. Source Settings



10.6. Diagnostic



10.7. USB Operations

USB operations option can not be used directly. It can be used for updating panel tool, hw congiguration etc.

11. SOFTWARE UPDATE

In MB61 project there is only one software. From following steps software update procedure can be seen:

1. MB61_en.bin, mboot.bin and usb_auto_update_T4.txt documents should copy directly inside of a flash memory(not in a folder).
2. Put flash memory to the tv when tv is powered off.
3. Power on the and wait when the tv is opened.
4. If First Time Installition screen comes, it means software update procedure is succesful.

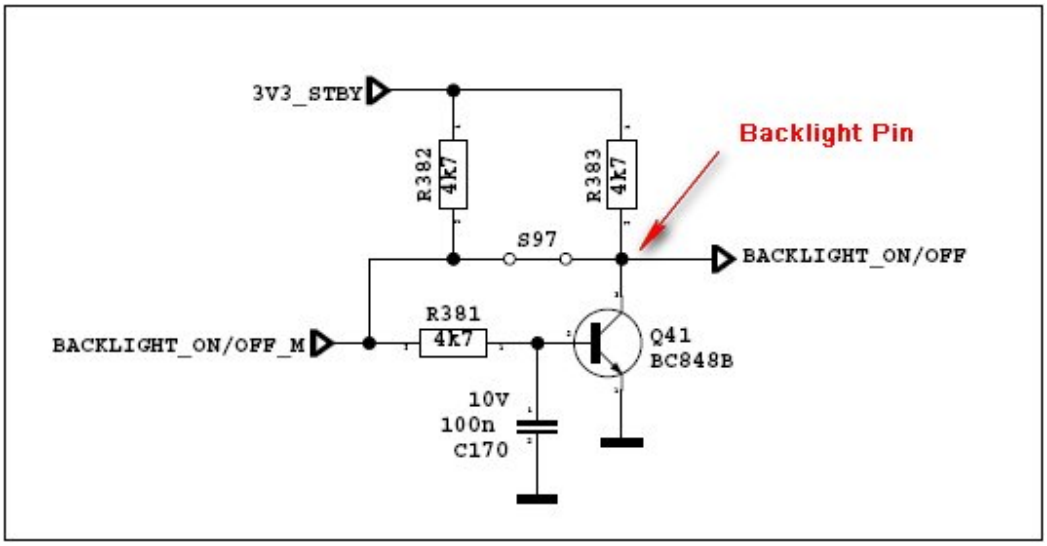
12. TROUBLESHOOTING

12.1. No Backlight Problem

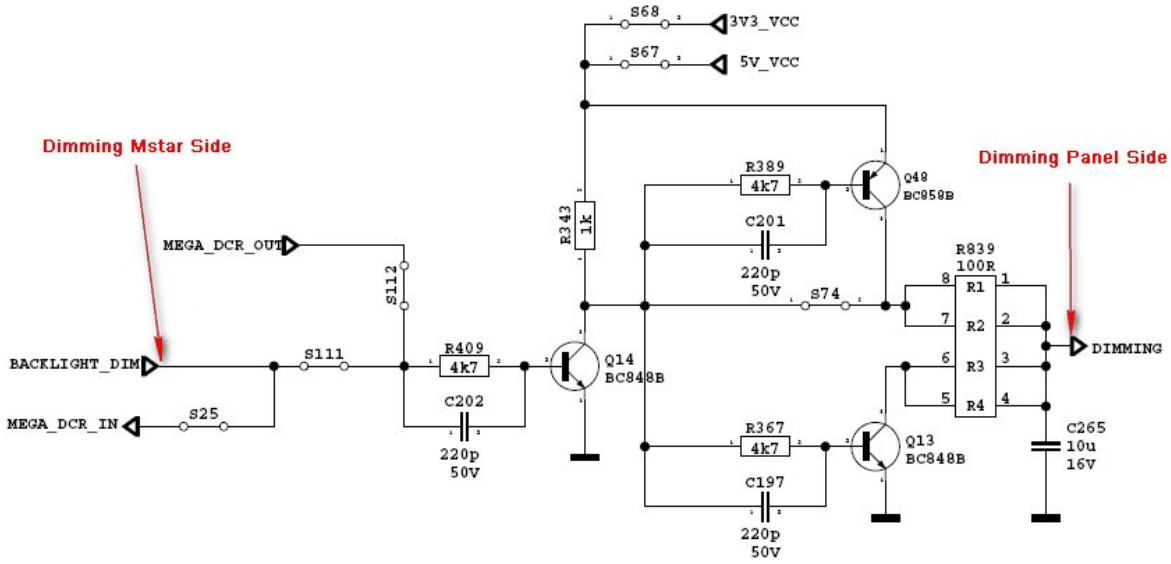
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible couses: Backlight pin, dimming pin, backlight supply, stby on/off pin

Backlight pin should be high in open position. If it is low, please check Q41 and panel cables.

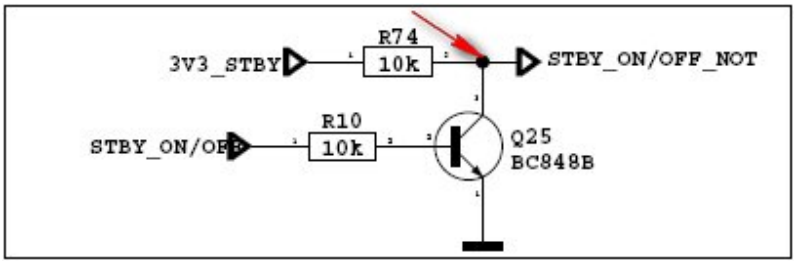


Dimming pin should be high or square wave in open position. If it is low, please check S111 for Mstar side and panel or power cables,
connectors.



Backlight power supply should be in panel specs.

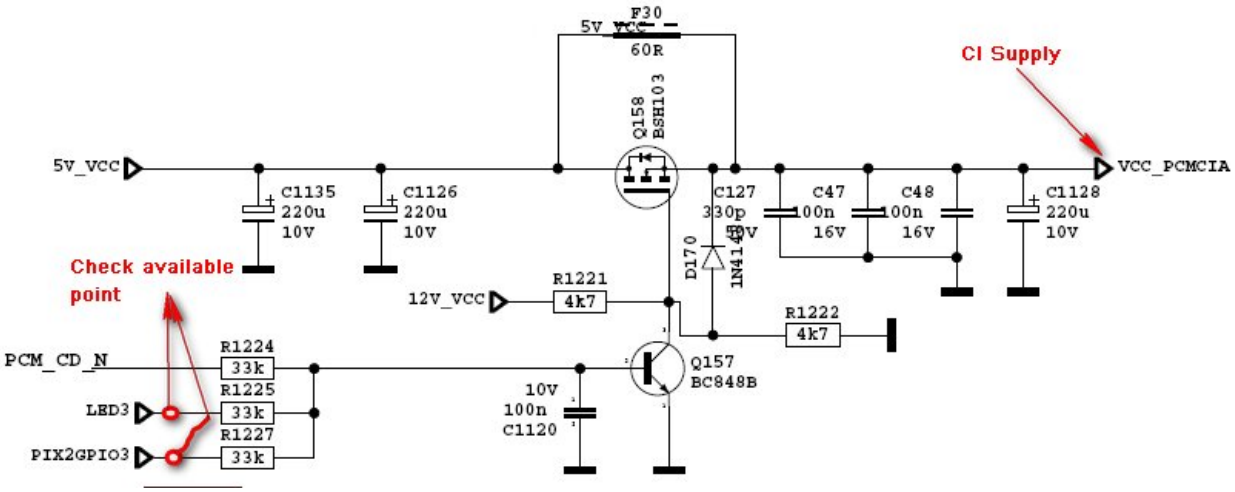
STBY_ON/OFF should be low for standby on condition, please check R74.



12.2. CI Module Problem

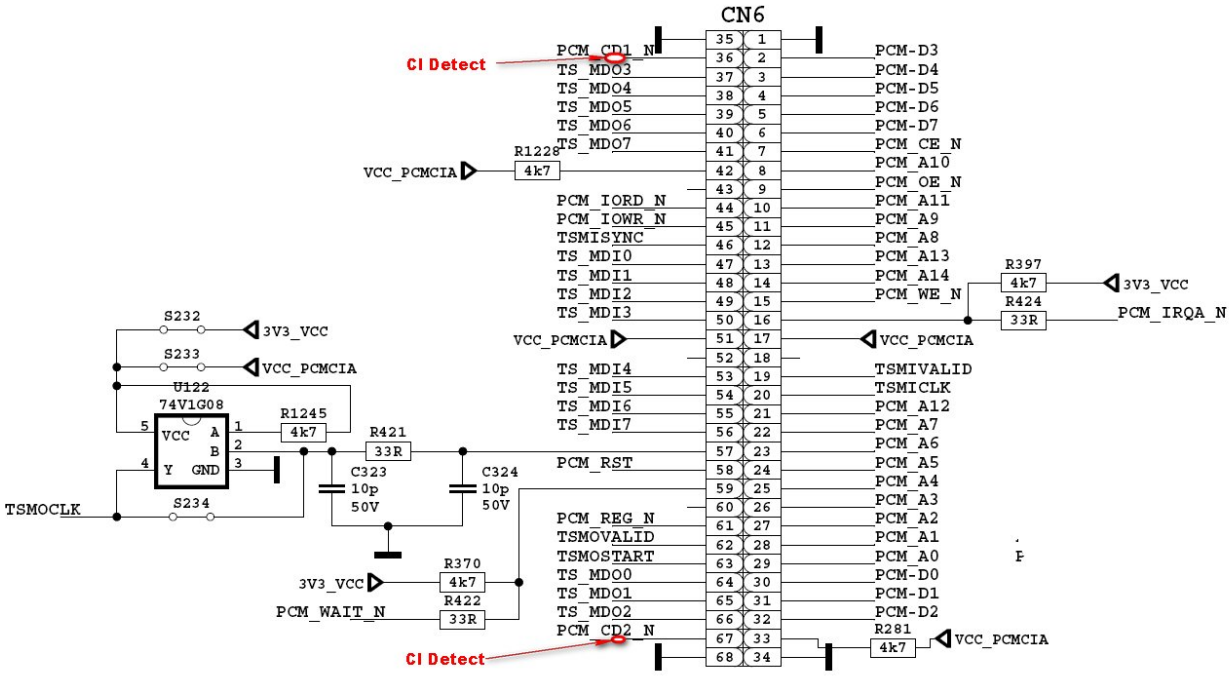
Problem: CI is not working when CI module inserted.

Possible couses: Supply, suply control pin, detect pins, mechanical positions of pins
CI supply shoul be 5V when CI module inserted. If it is not 5V please check LED3 or PIX2 pin, this pin should be low.



Please check mechanical positions of CI module.

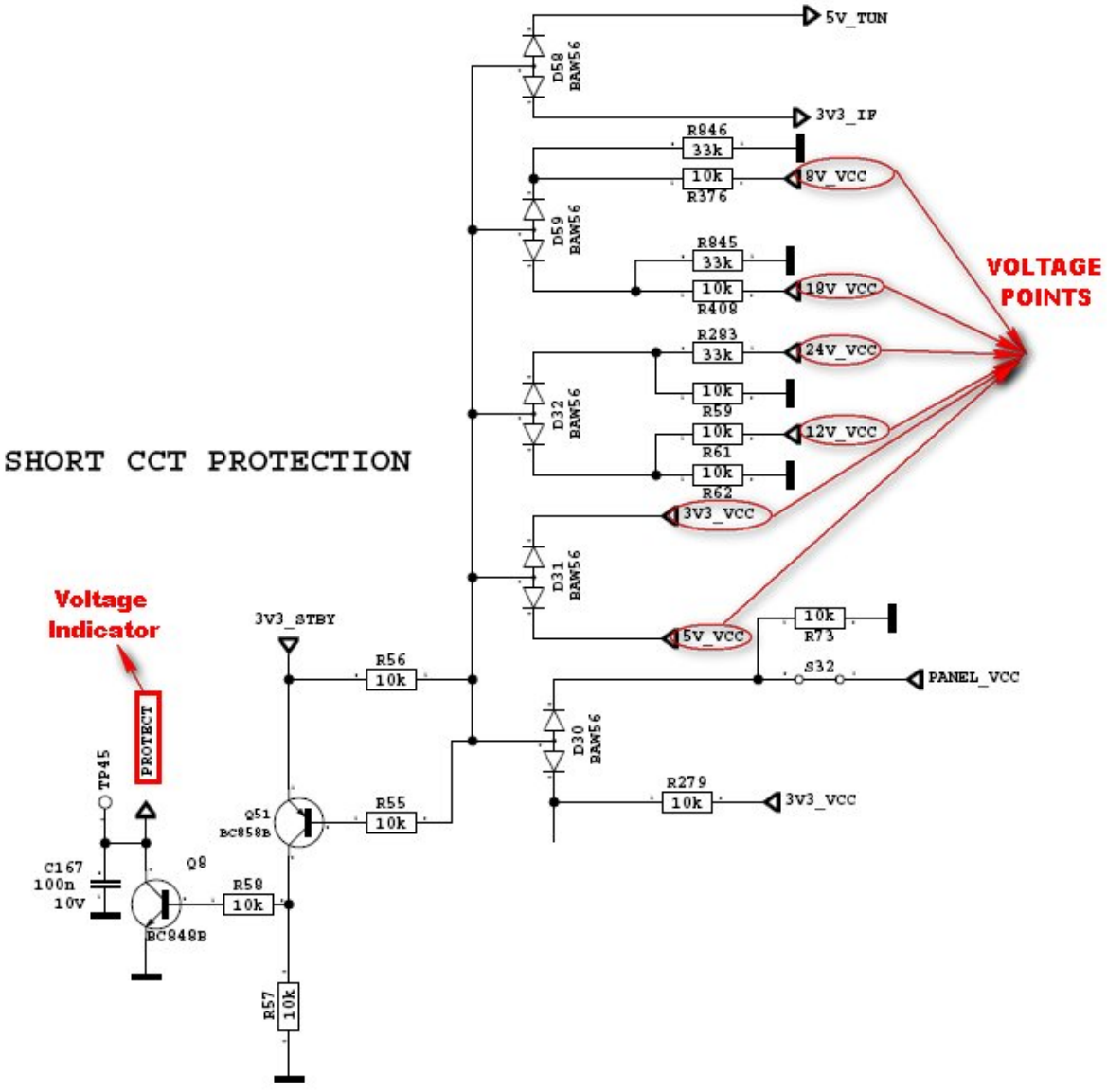
Detect ports should be low. If it is not low please check CI connector pins, CI module pins and 3V3_VCC on MB61.


CN6
CI Detect
PCM_CD1_N
TS_MDO3
TS_MDO4
TS_MDO5
TS_MDO6
TS_MDO7
R1228
4k7
VCC_PCMCIA
PCM_IORD_N
PCM_IOWR_N
TSMISYNC
TS_MDI0
TS_MDI1
TS_MDI2
TS_MDI3
VCC_PCMCIA
TS_MDI4
TS_MDI5
TS_MDI6
TS_MDI7
PCM_RST
PCM_REG_N
TSMOVALID
TSMOSTART
TS_MDO0
TS_MDO1
TS_MDO2
PCM_CD2_N
CI Detect
PCM-D3
PCM-D4
PCM-D5
PCM-D6
PCM-D7
PCM_CE_N
PCM_A10
PCM_OE_N
PCM_A11
PCM_A9
PCM_A8
PCM_A13
PCM_A14
PCM_WE_N
R397
4k7
3V3_VCC
R424
33R
PCM_IRQA_N
VCC_PCMCIA
TSMIVALID
TSMICLK
PCM_A12
PCM_A7
PCM_A6
PCM_A5
PCM_A4
PCM_A3
PCM_A2
PCM_A1
PCM_A0
PCM-D0
PCM-D1
PCM-D2
R281
4k7
VCC_PCMCIA
S232
3V3_VCC
S233
VCC_PCMCIA
U122
74V1G08
VCC
A
B
Y
GND
R1245
4k7
R421
33R
C323
10p
50V
C324
10p
50V
S234
TSMOCLK
3V3_VCC
R370
4k7
PCM_WAIT_N
R422
33R

12.3. Led Blinking Problem

Problem: LED blinking, no other operation

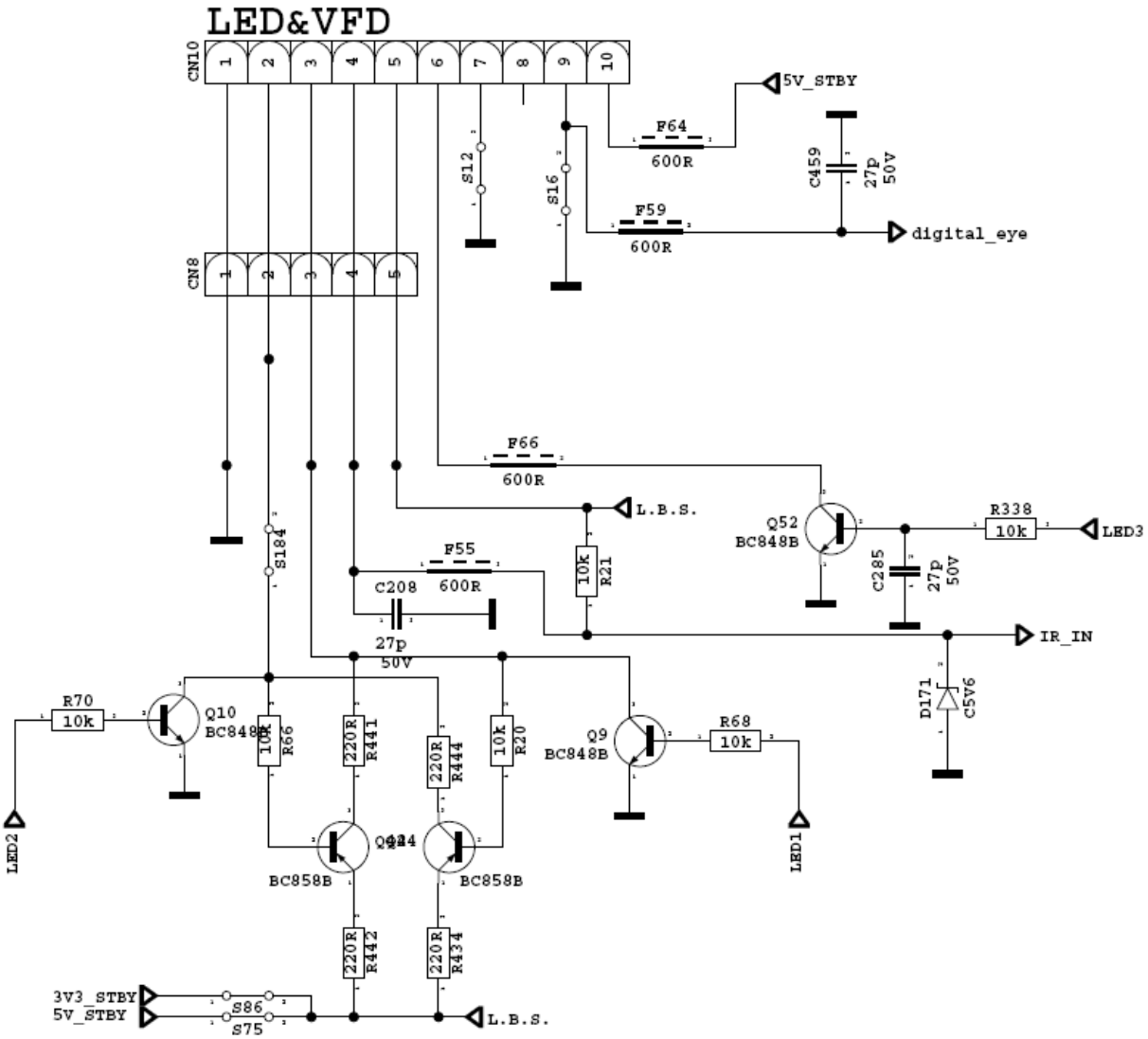
This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



12.4. IR Problem

Problem: LED or IR not working

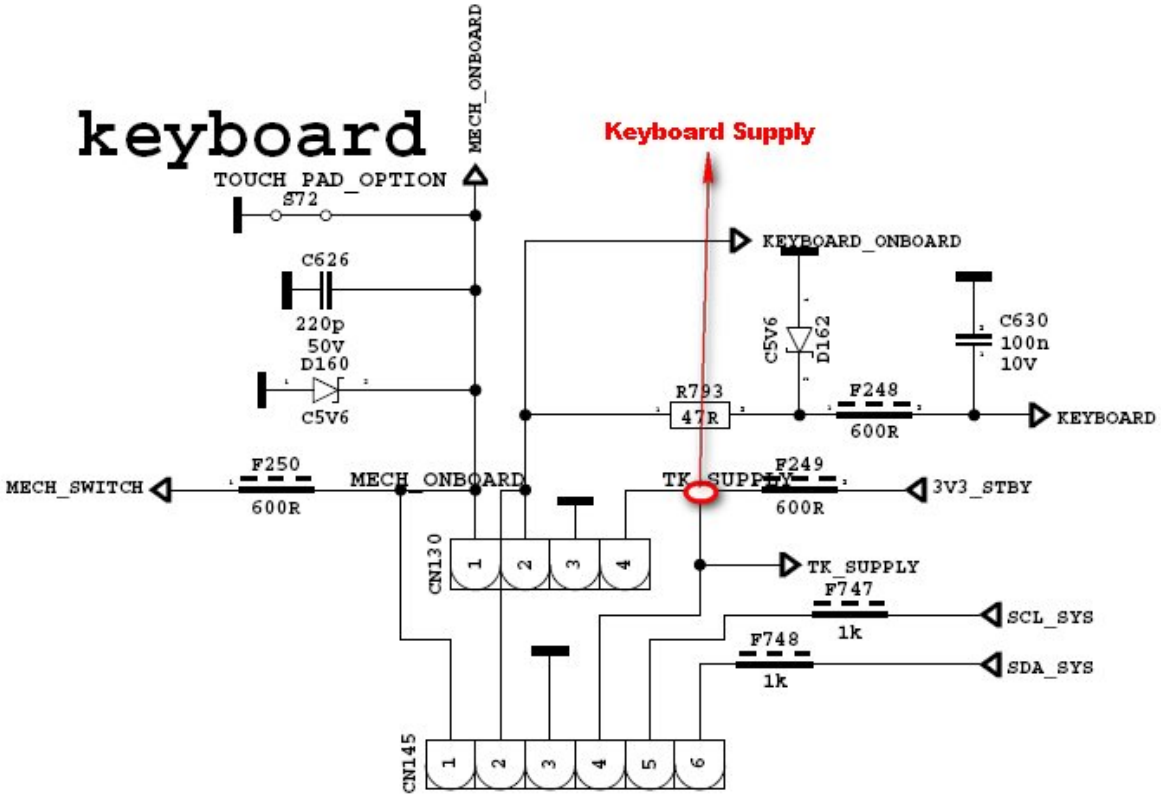
Check LED card supply on MB61 chasis.



12.5. Keypad Touchpad Problems

Problem: Keypad or Touchpad is not working

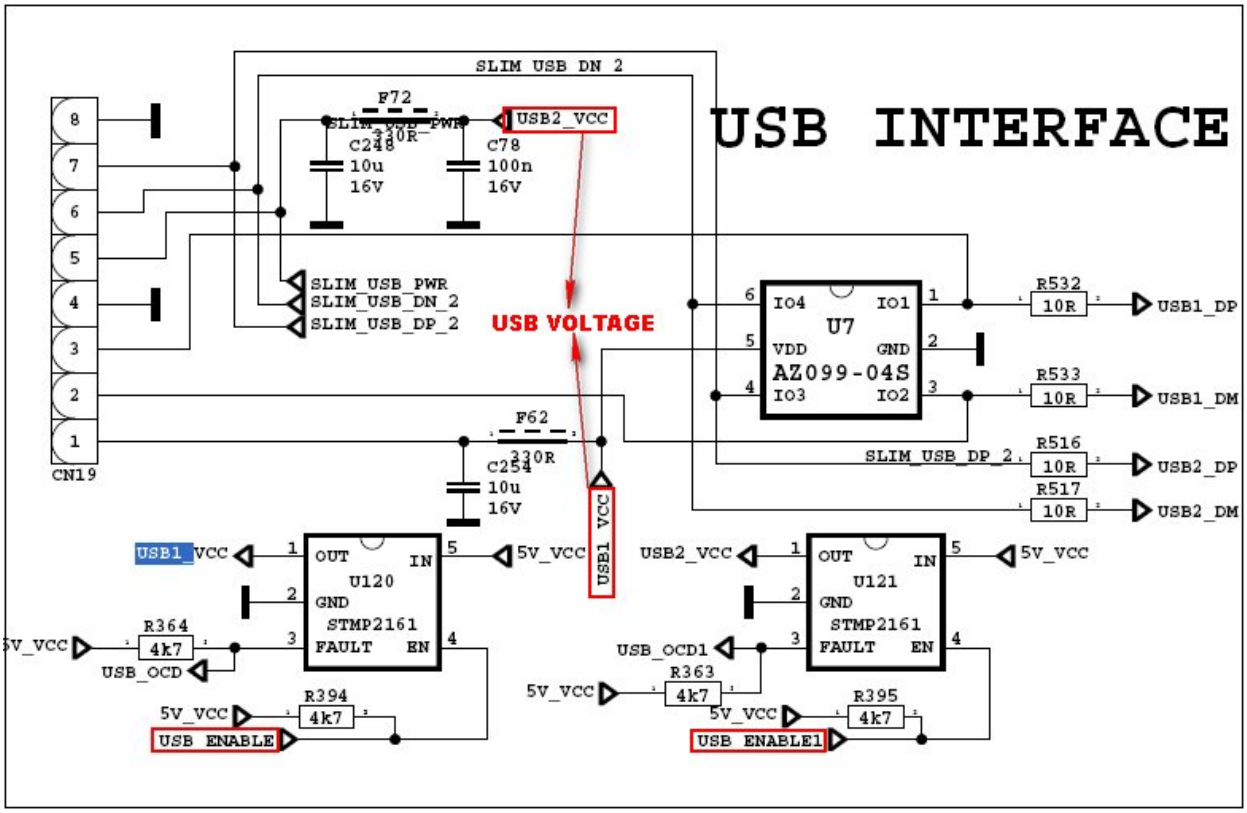
Check keypad supply and KEYBOARD pin on MB61.



12.6. USB Problems

Problem: USB is not working or no USB Detection.

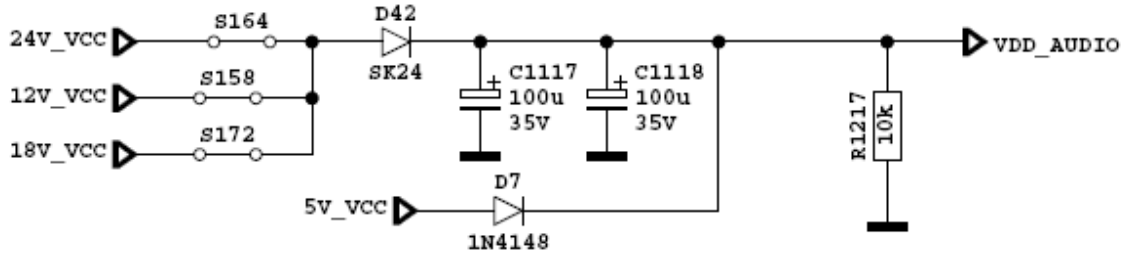
Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.



12.7. No Sound Problem

Problem: No audio at main TV speaker outputs.

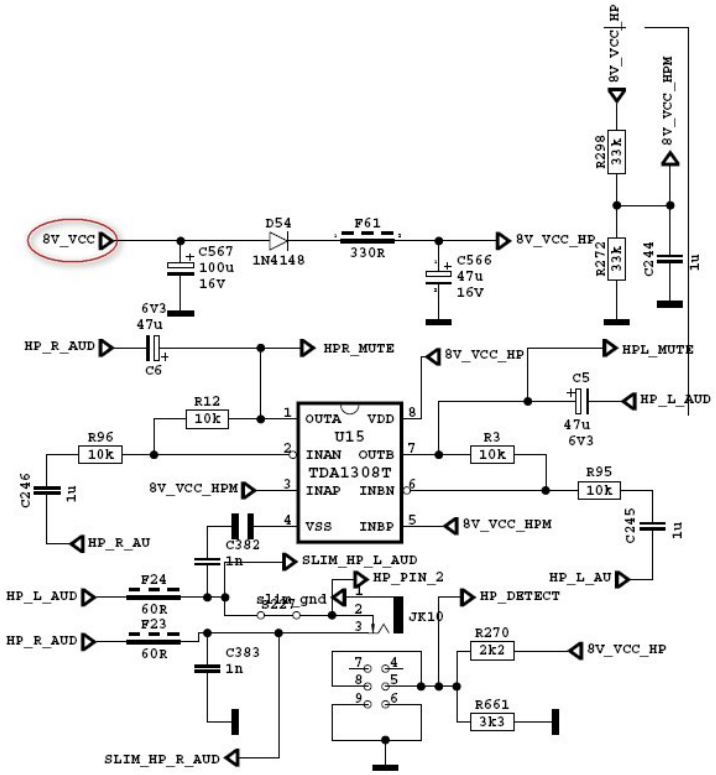
Check supply voltages of VDD_AUDIO, 5V_VCC and 3V3_VCC with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



12.8. No Sound Problem at Headphone

Problem: No audio at headphone output.

Check HP detect pin, when headphone is. Check 8V_VCC with a voltage-meter.



12.9. Standby On/Off Problem

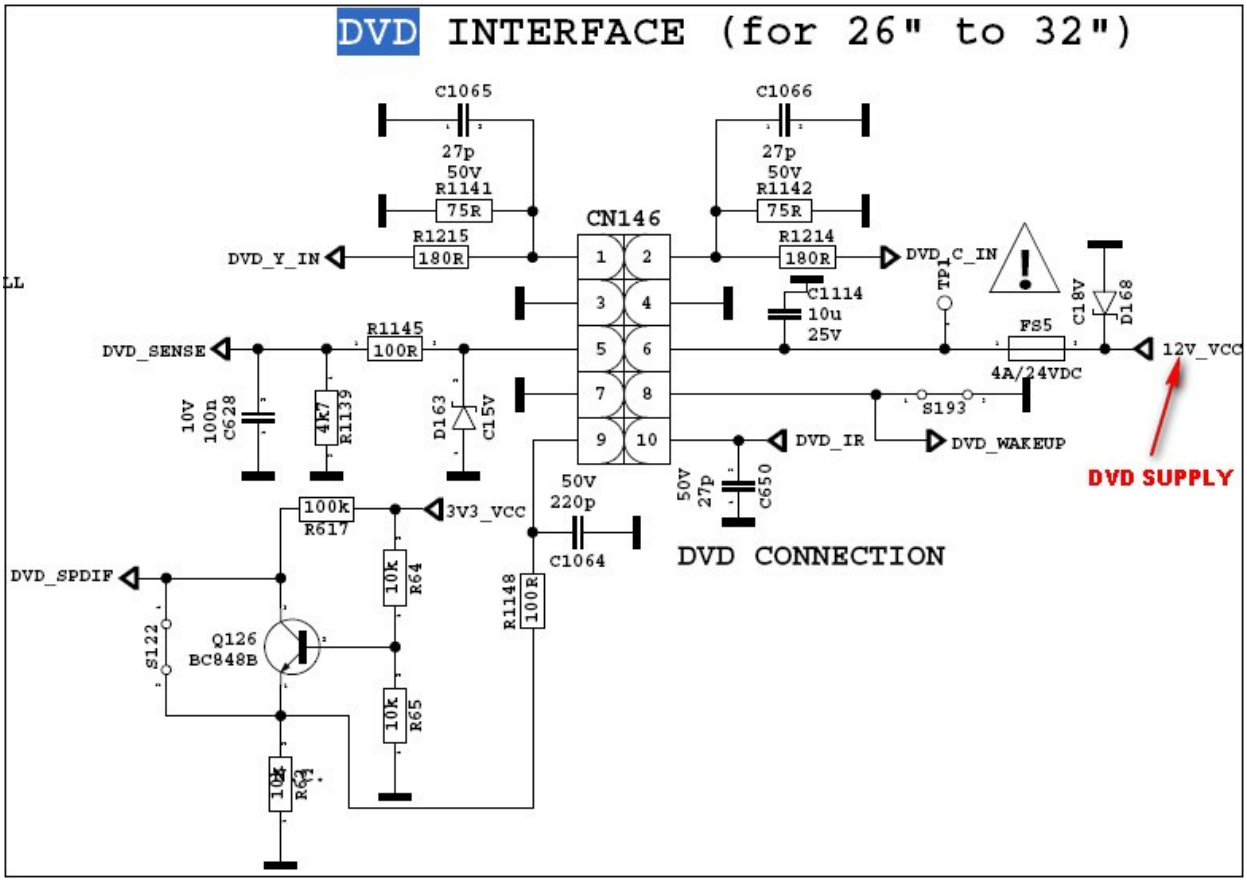
Problem:
Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check 12V_VCC, 5V_VCC and 3V3_VCC with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via hyper-terminal (or Teraterm). These printouts may give a clue about the problem.

DVD Problems

Problem: DVD is not working.

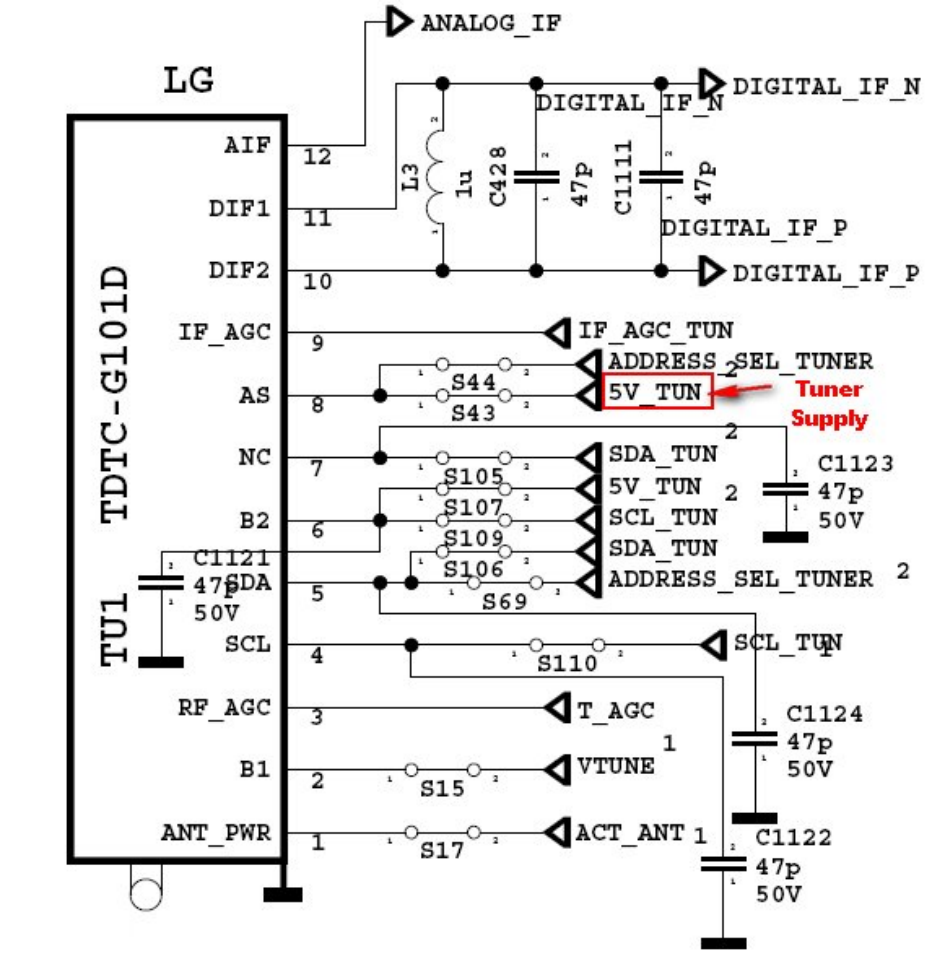
Check that DVD source is selected in Service menu. Check supply voltage of DVD namely 12V_VCC.



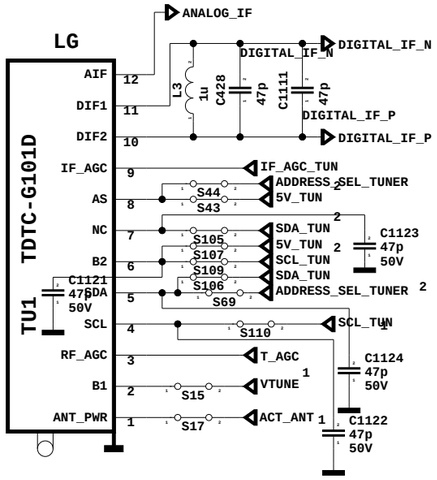
12.10. No Signal Problem

Problem: No signal in TV mode.

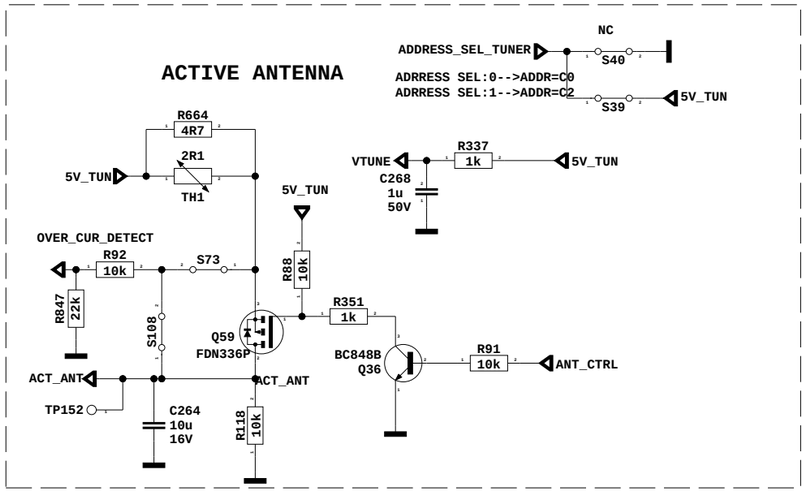
Check tuner supply voltage; 5V_TUN. Check tuner options are correctly set in Service menu. Check AGC voltage at RF_AGC pin of tuner.

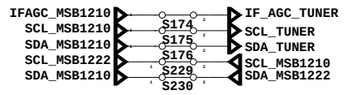


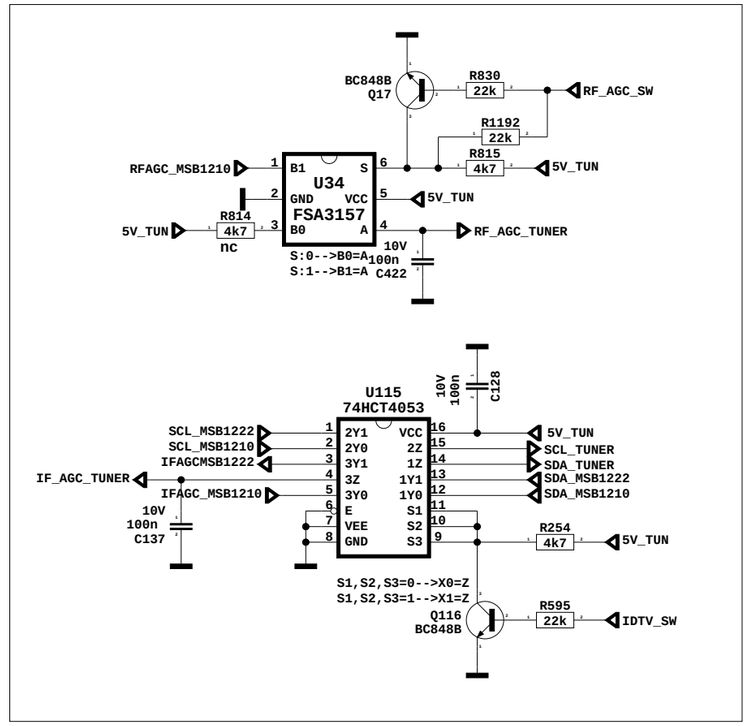
Samsung/Ntune

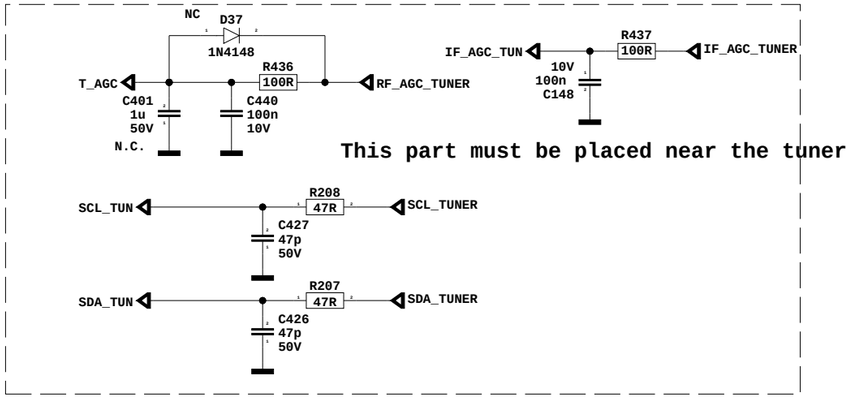


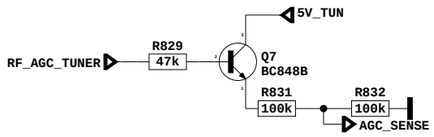
Samsung/Ntune

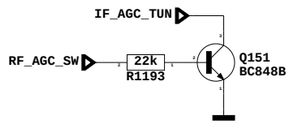


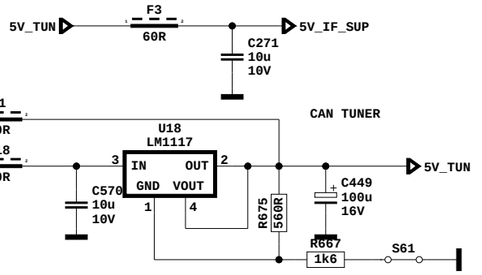


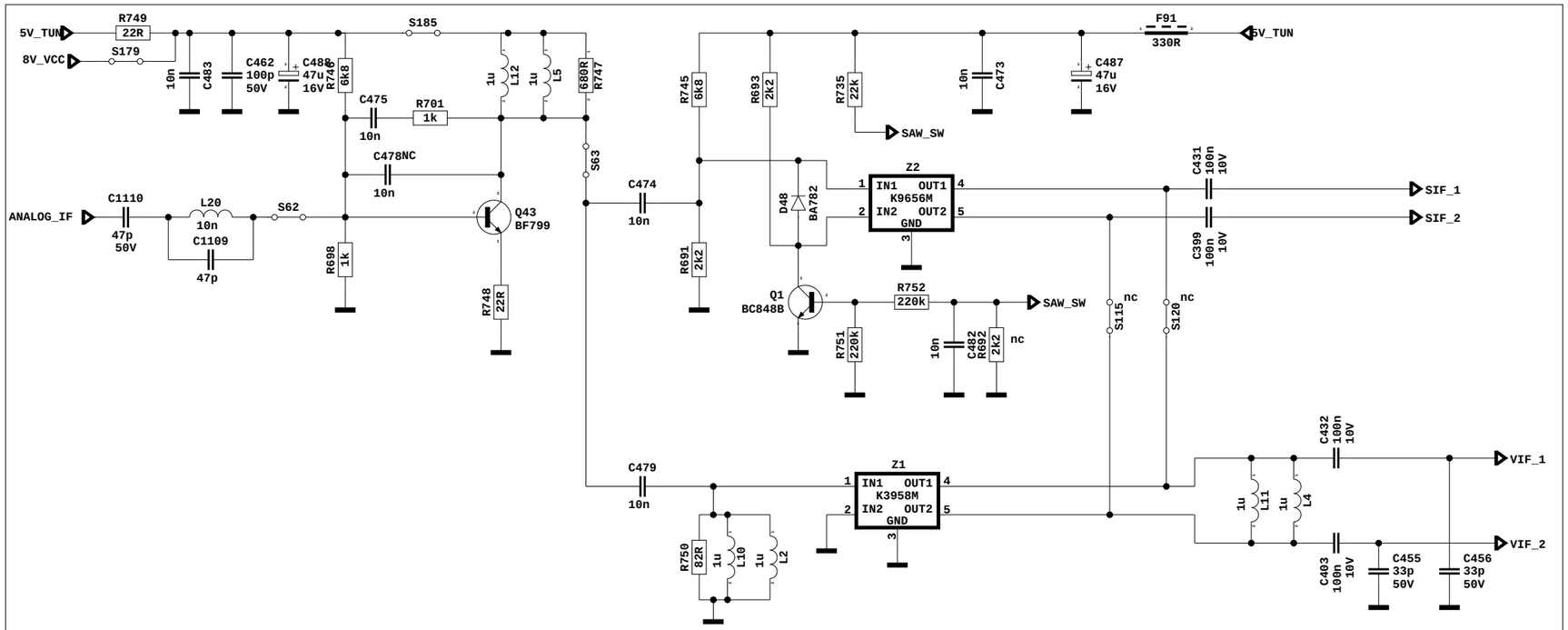


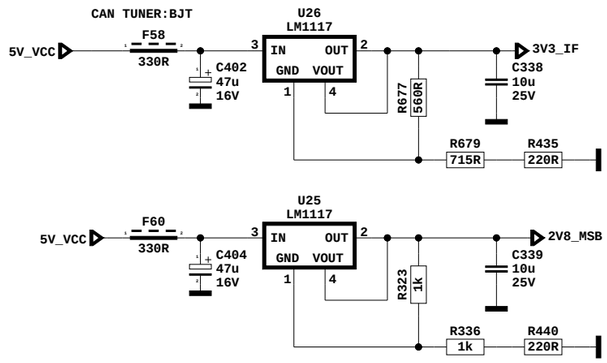












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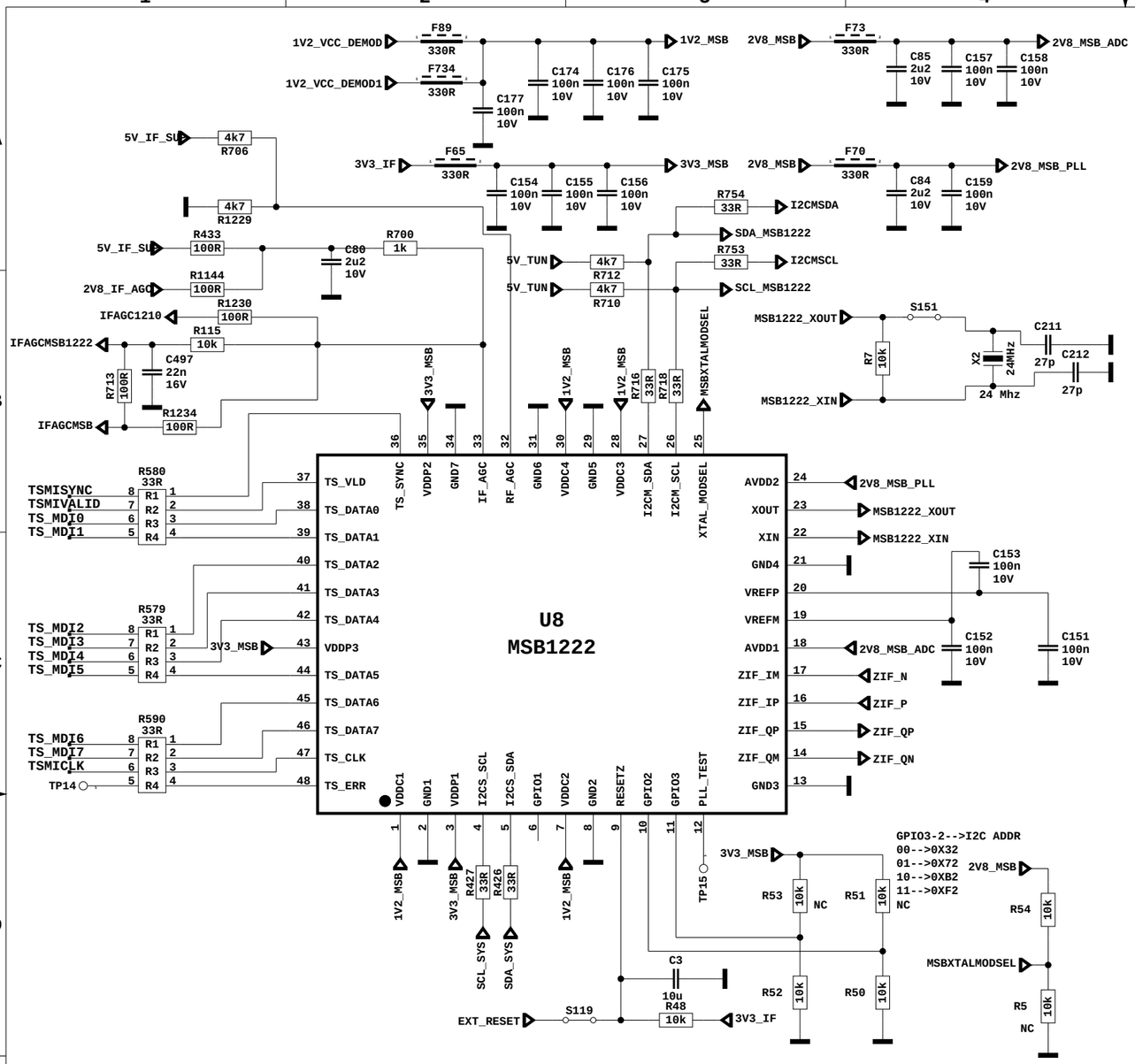
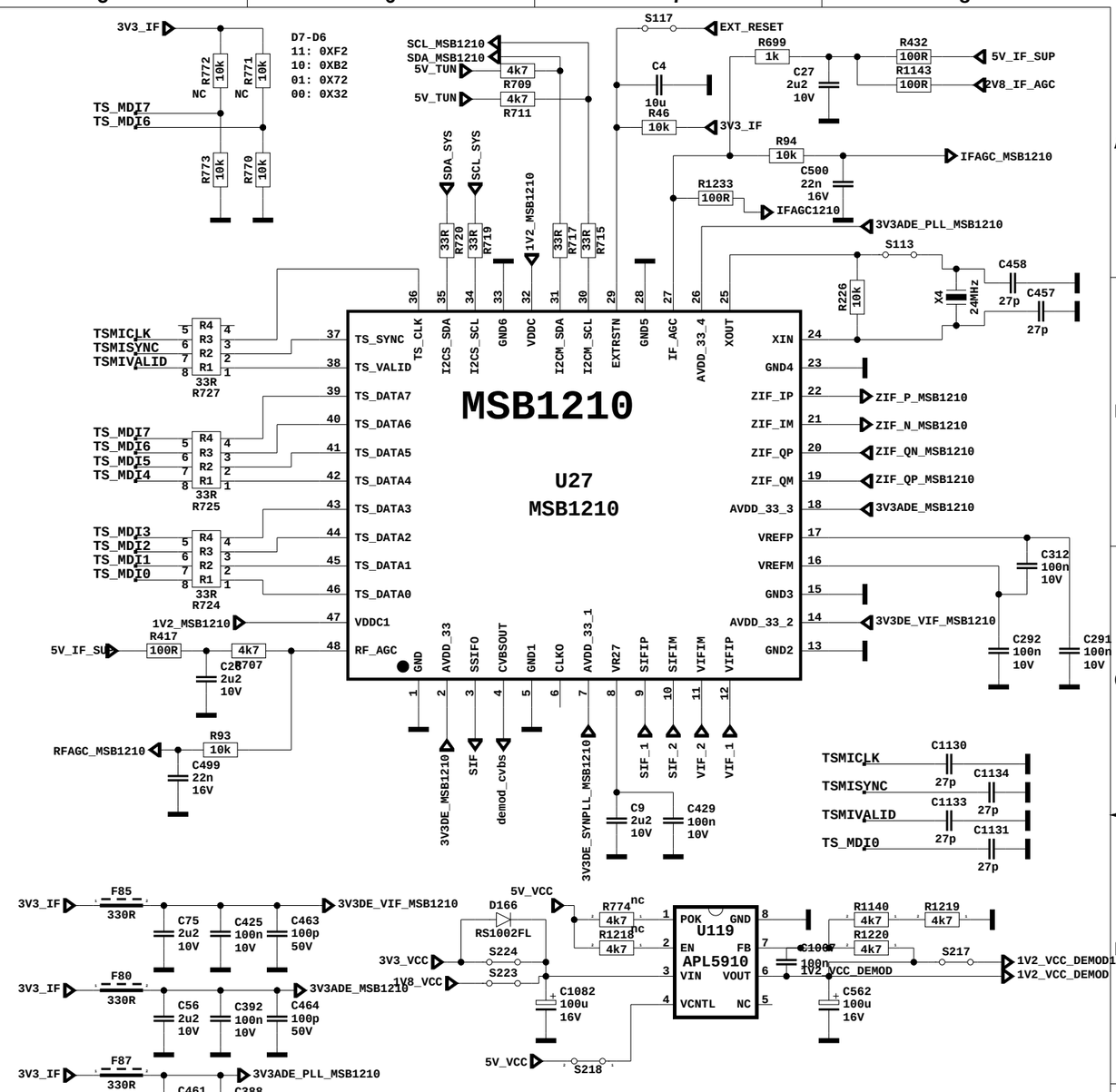
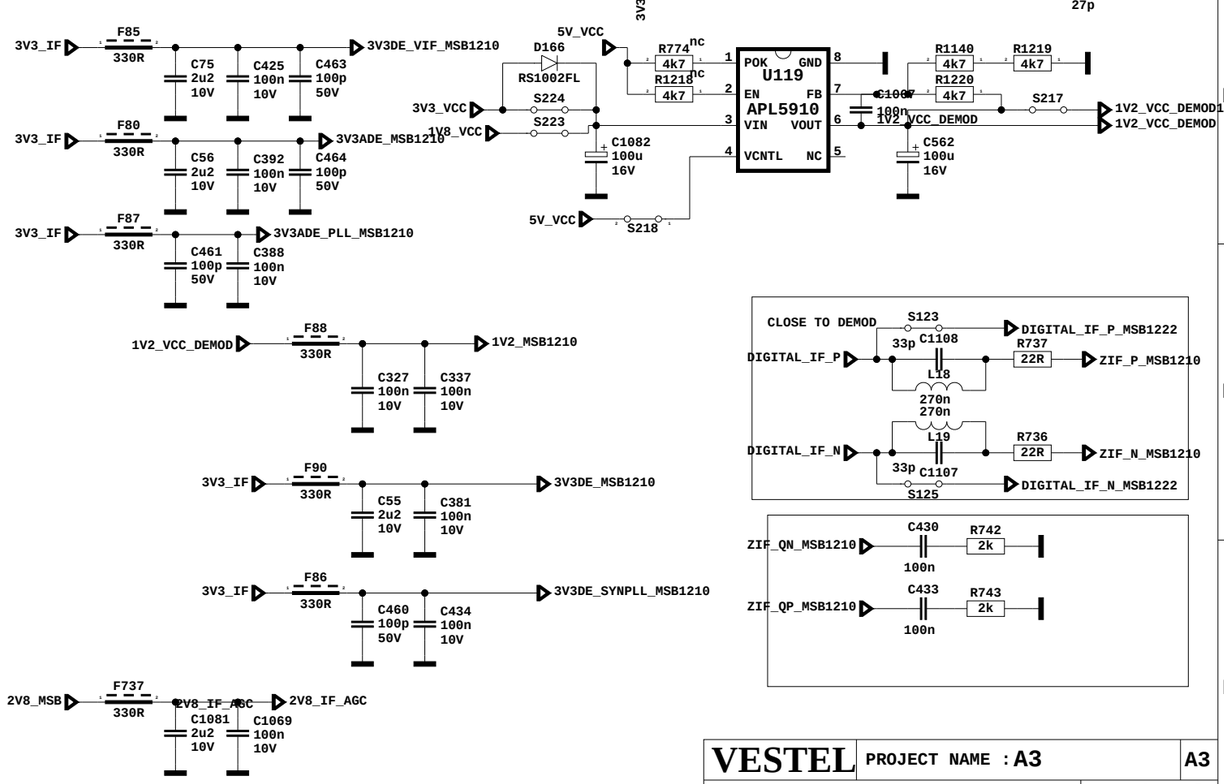
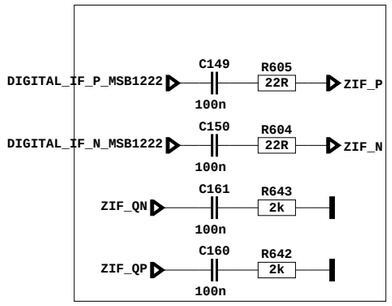
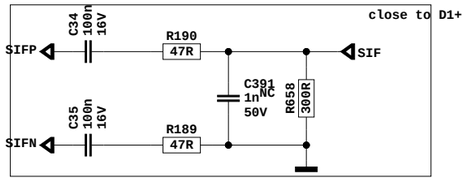
DRAWN BY :<YOUR NAME HERE>	12-01-2010_13:22	

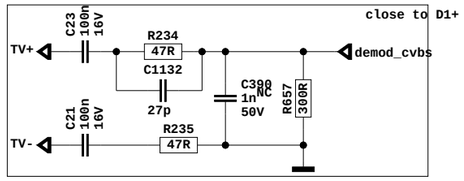












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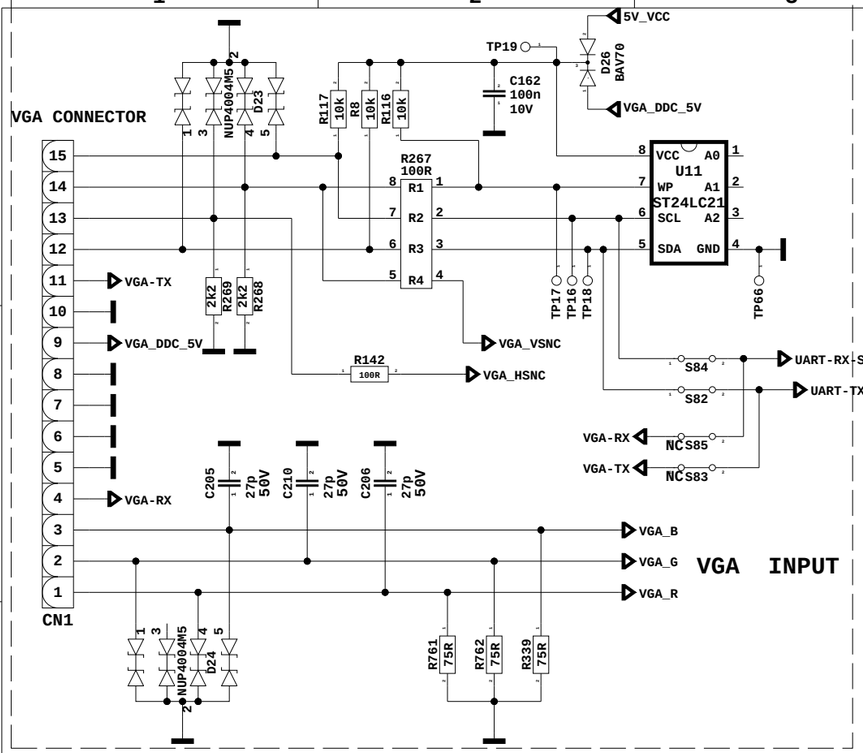
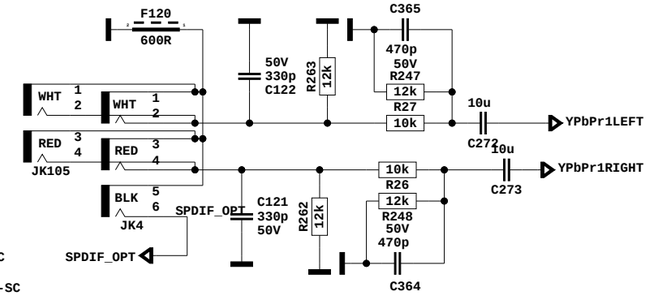
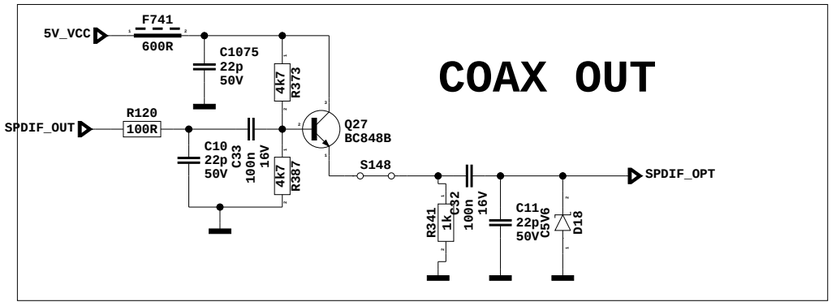
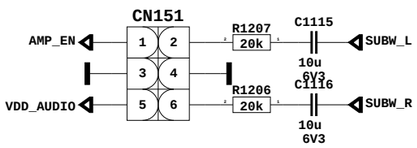
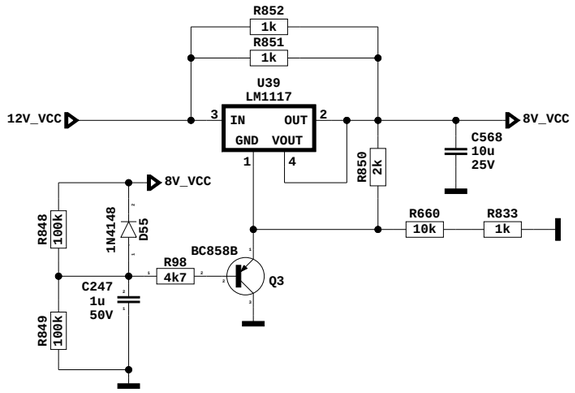
DRAWN BY :<YOUR NAME HERE>		11-01-2010_13:31

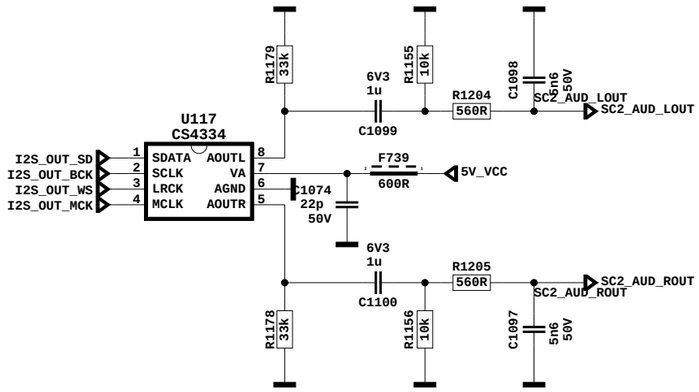


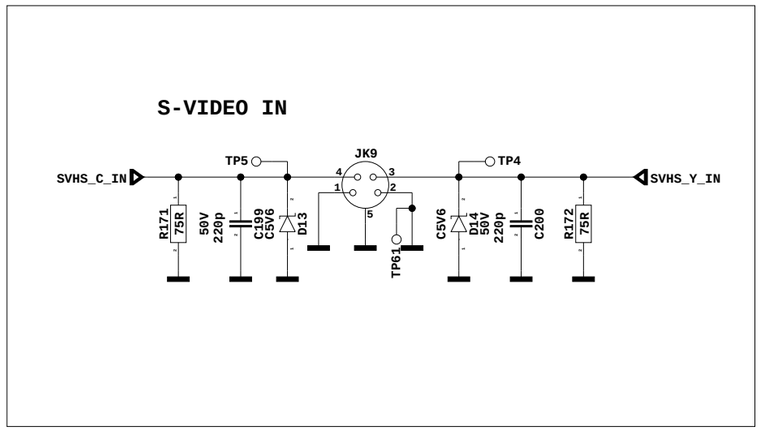


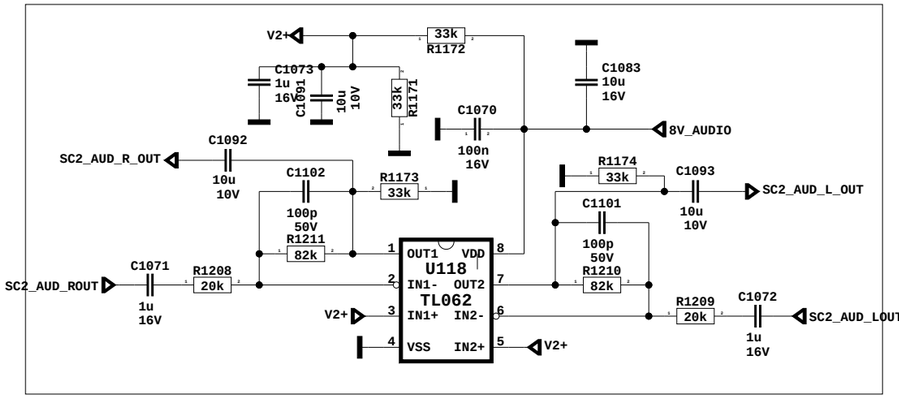












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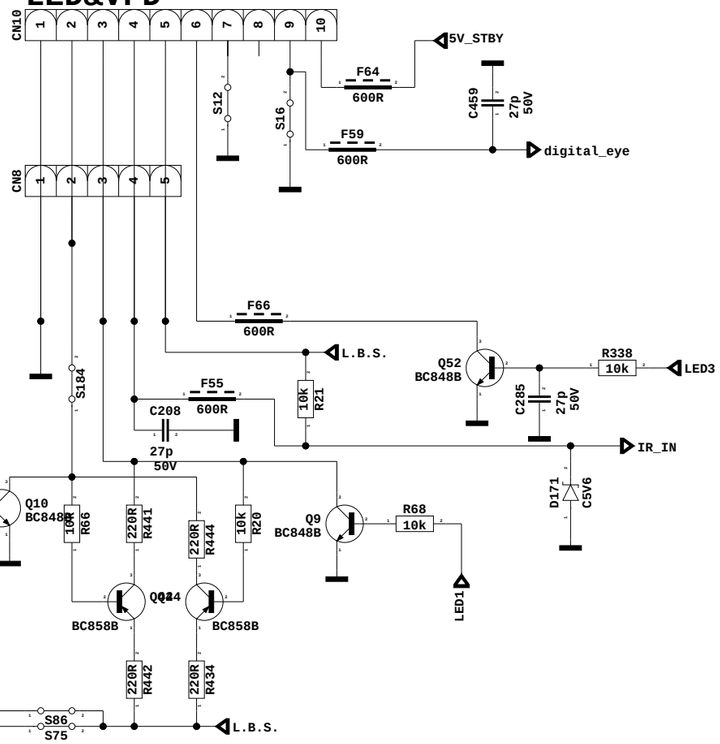
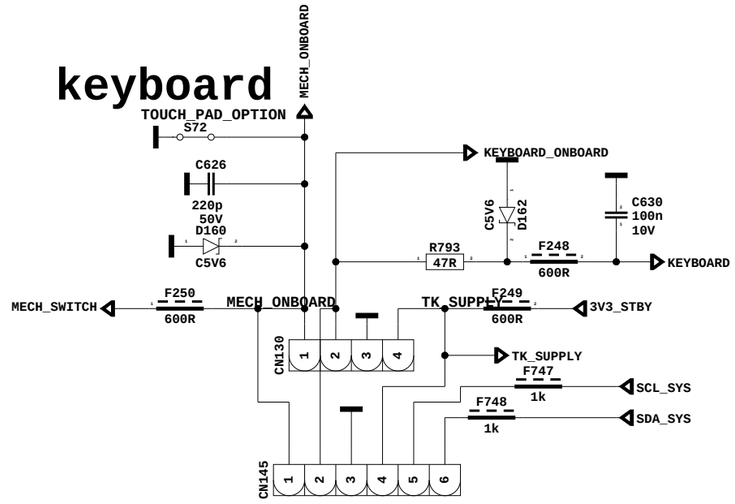
DRAWN BY : <YOUR NAME HERE>	11-01-2010_09:54	

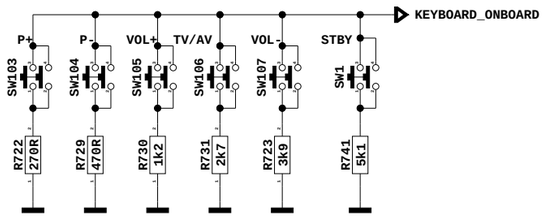
LED&VFD



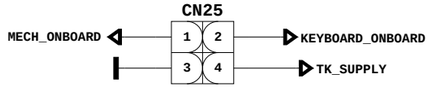
keyboard



PUSH V+ AND V- AT THE SAME TIME FOR MENU



CN25



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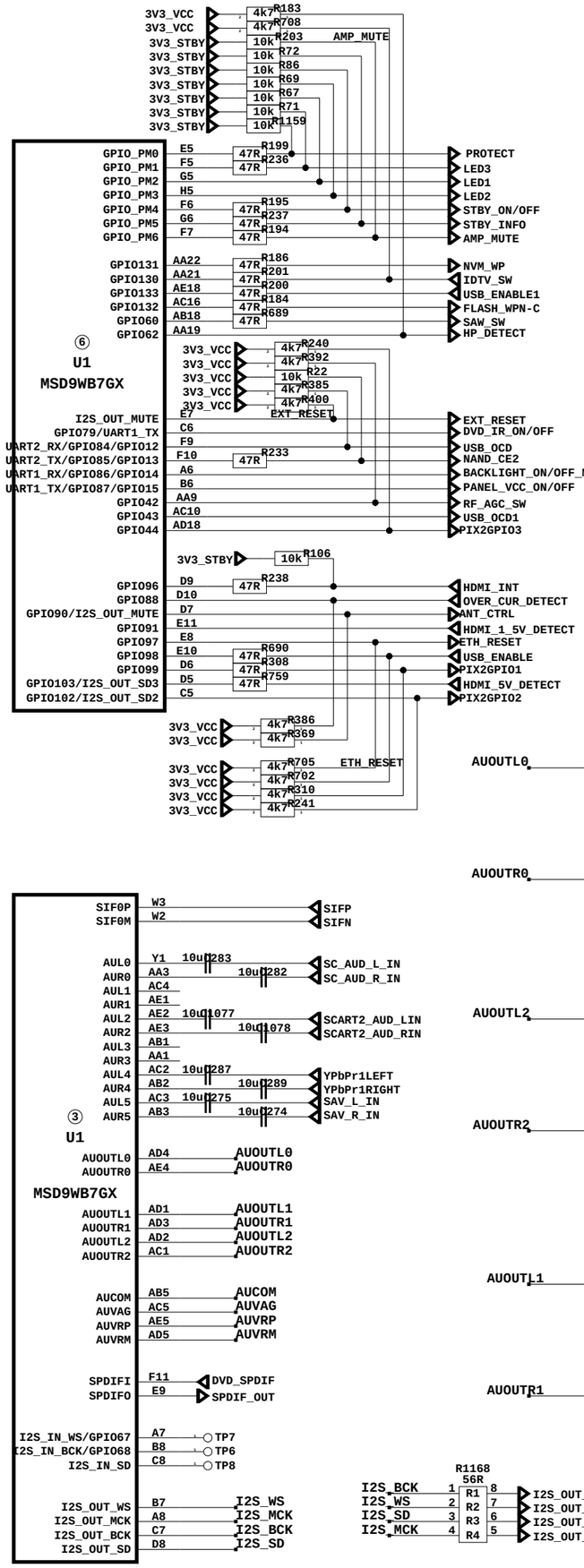

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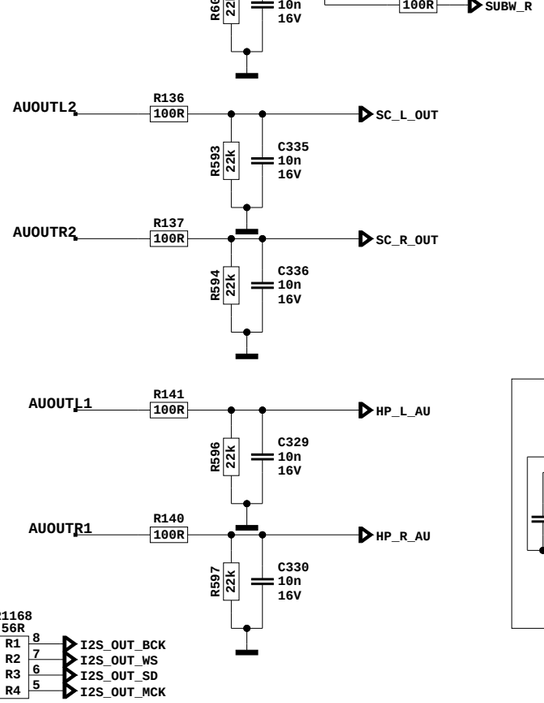

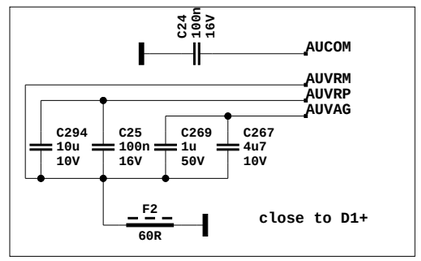

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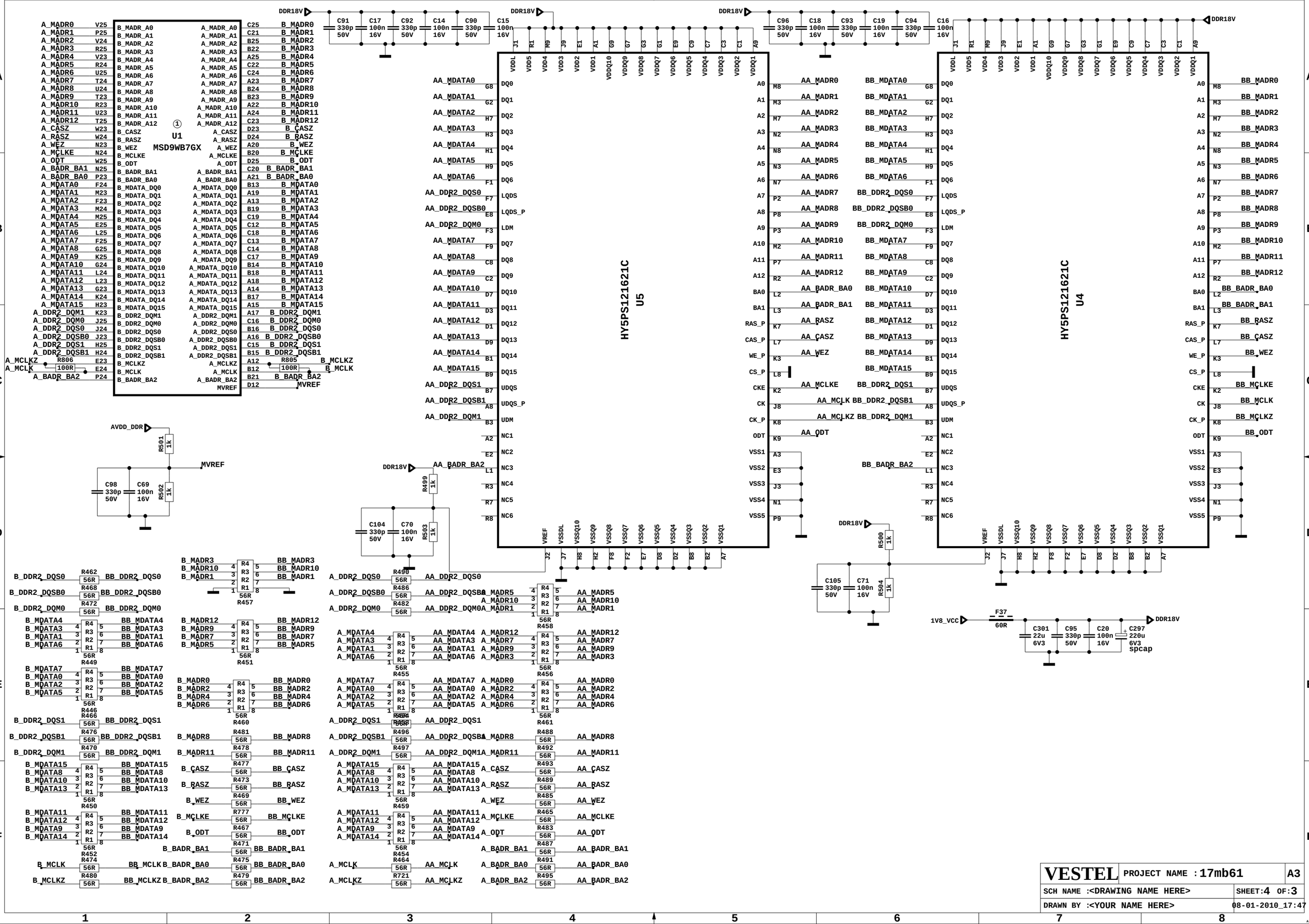
DRAWN BY :<YOUR NAME HERE>	11-01-2010_14:57	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U5
HY5PS121621C
U4
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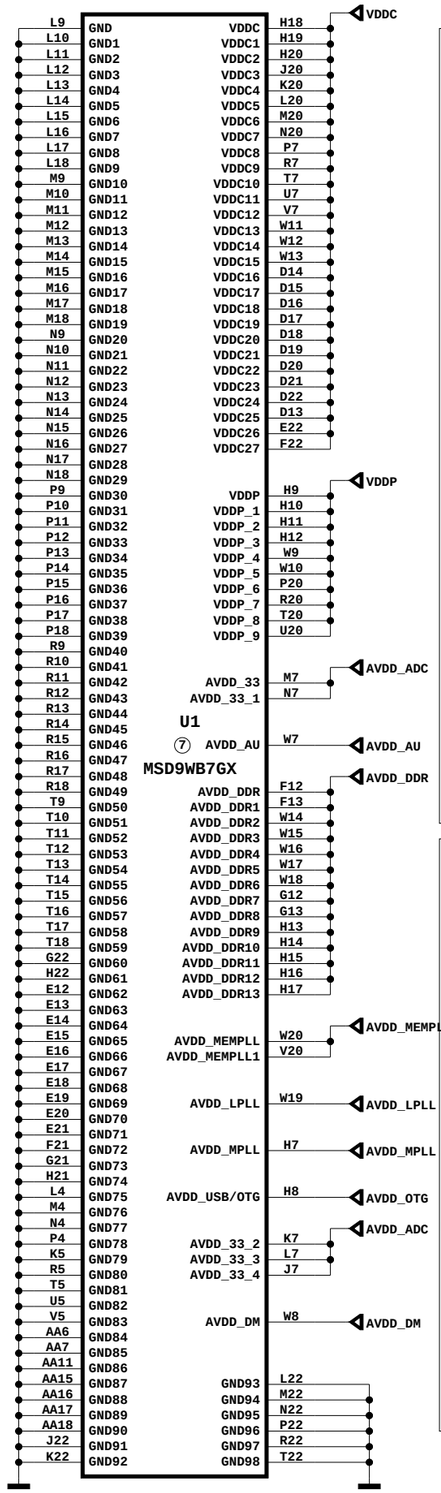
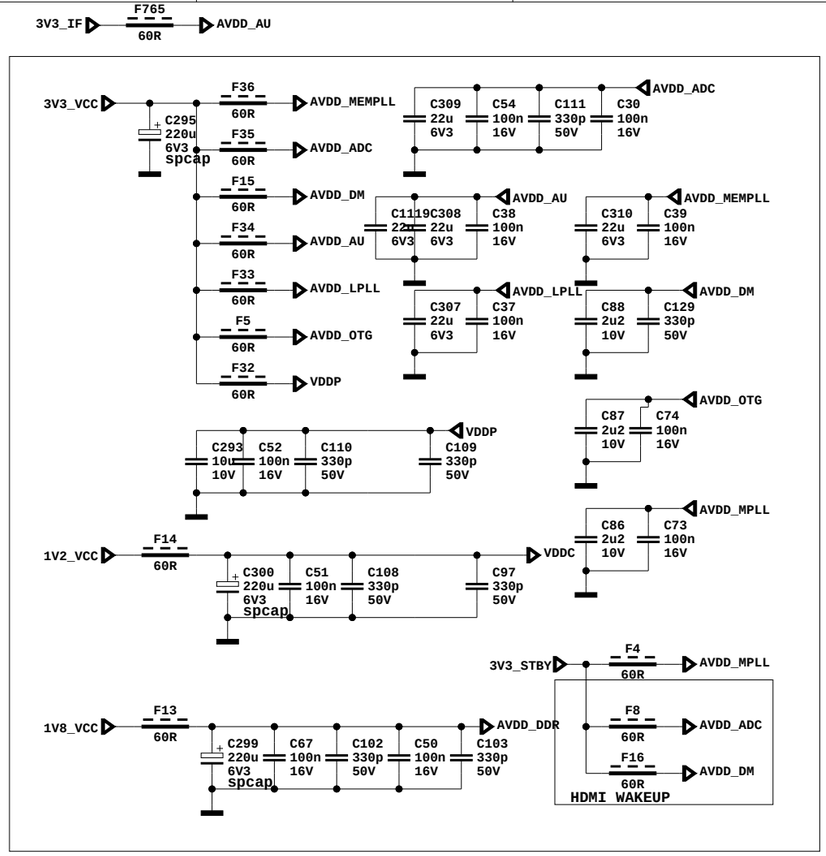
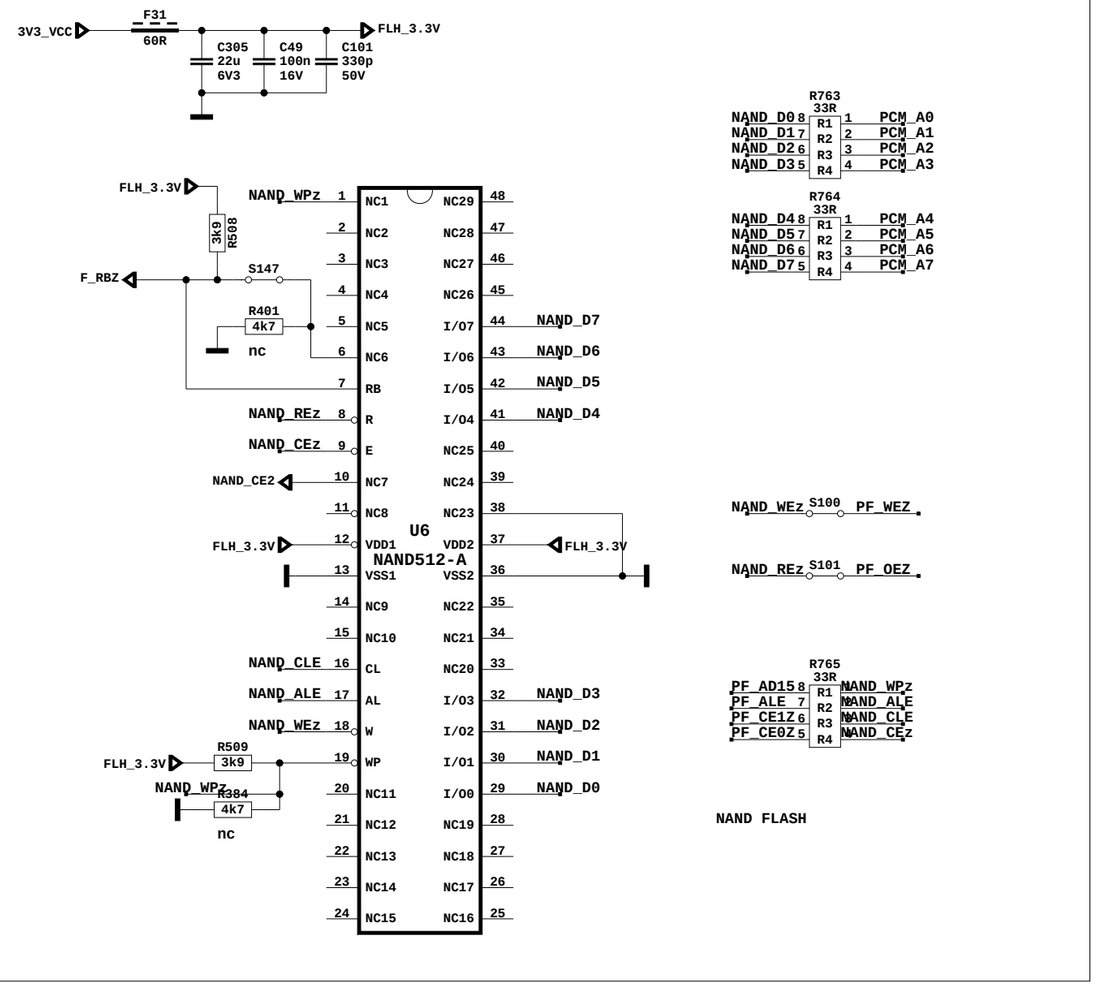
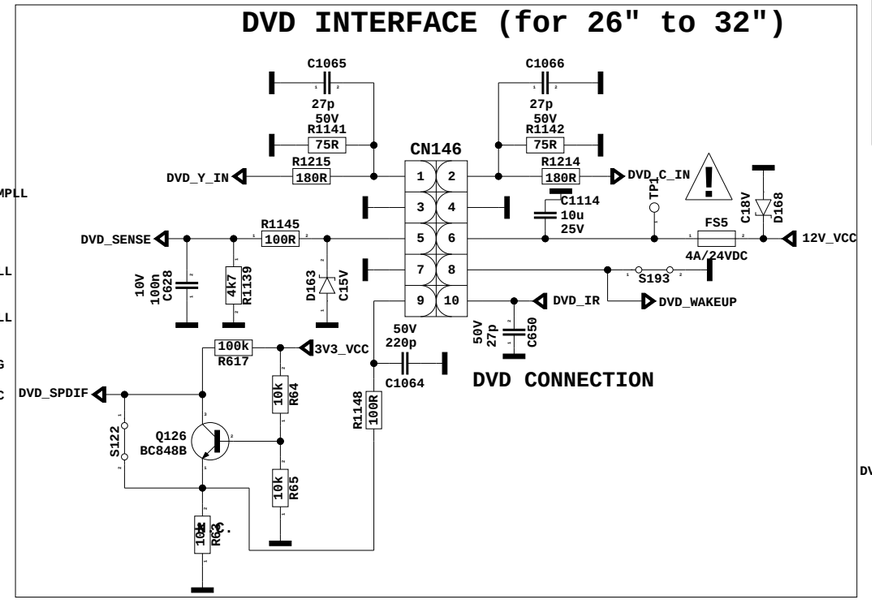
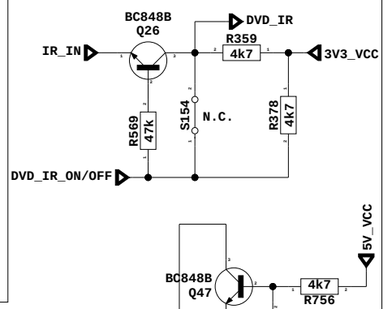
AVDD_DDR
MVREF
1V8_VCC
VESTEL
PROJECT NAME :17mb61
A3
SCH NAME :<DRAWING NAME HERE>
SHEET:4 OF:3
DRAWN BY :<YOUR NAME HERE>
08-01-2010_17:47

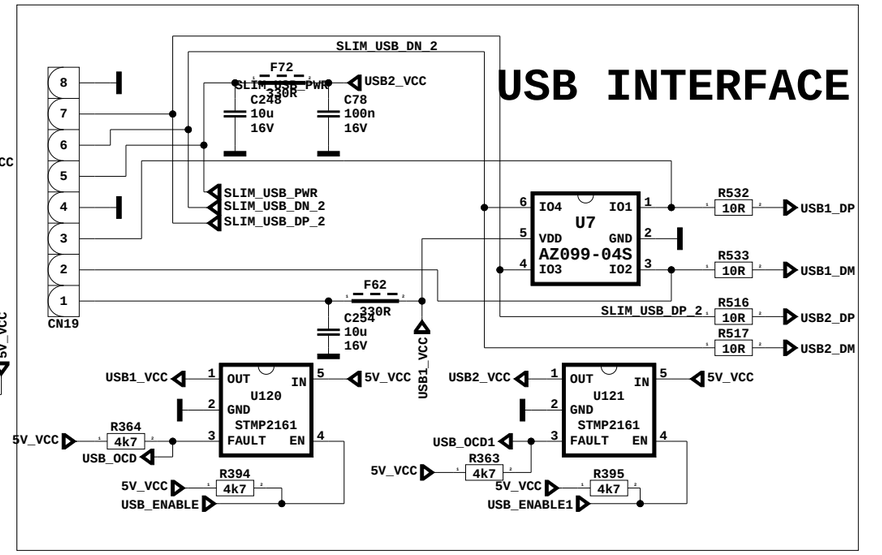


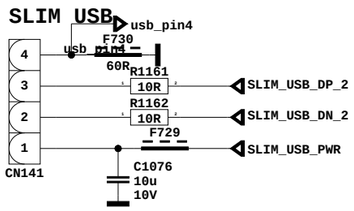


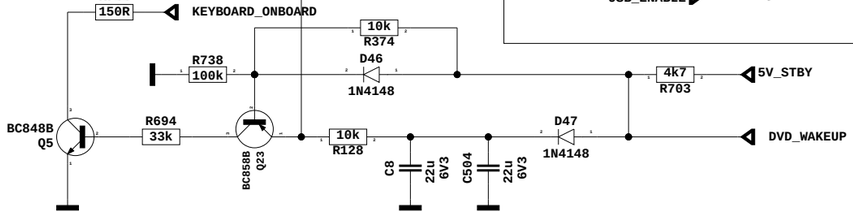












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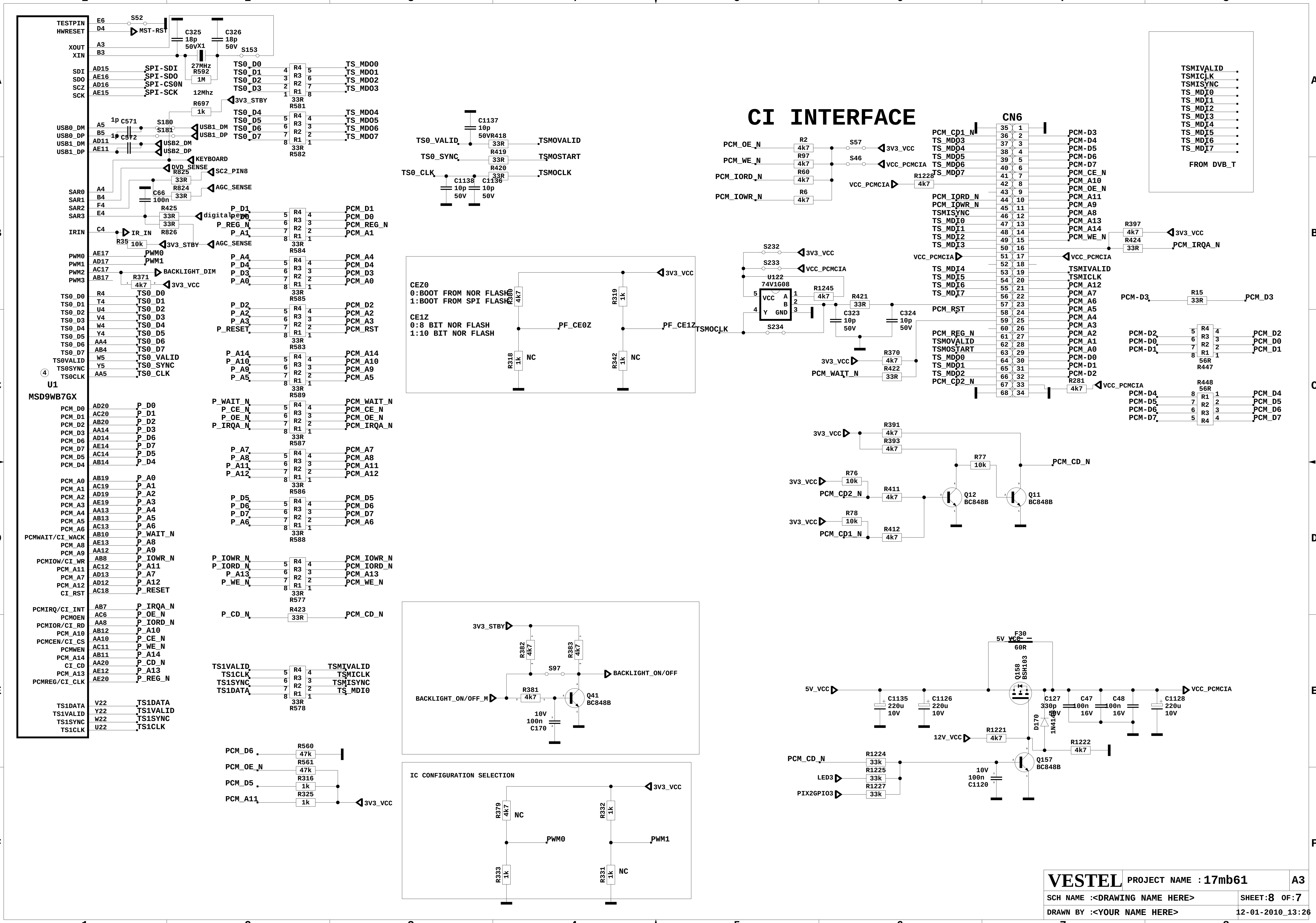
DRAWN BY : <YOUR NAME HERE>	11-01-2010_09:20	



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HWRESET
XOUT
XIN
SDI
SDO
SCZ
SCK
USB0_DM
USB0_DP
USB1_DM
USB1_DP
SAR0
SAR1
SAR2
SAR3
IRIN
PWM0
PWM1
PWM2
PWM3
TS0_D0
TS0_D1
TS0_D2
TS0_D3
TS0_D4
TS0_D5
TS0_D6
TS0_D7
TS0VALID
TS0SYNC
TS0CLK
PCM_D0
PCM_D1
PCM_D2
PCM_D3
PCM_D6
PCM_D7
PCM_D5
PCM_D4
PCM_A0
PCM_A1
PCM_A2
PCM_A3
PCM_A4
PCM_A5
PCM_A6
PCMWAIT/CI_WACK
PCM_A8
PCM_A9
PCMIOW/CI_WR
PCM_A11
PCM_A7
PCM_A12
CI_RST
PCMIRQ/CI_INT
PCMOEN
PCMIOR/CI_RD
PCM_A10
PCMCEN/CI_CS
PCMWEN
PCM_A14
CI_CD
PCM_A13
PCMREG/CI_CLK
TS1DATA
TS1VALID
TS1SYNC
TS1CLK
MST-RST
C325 18p 50V
C326 18p 50V
X1 27MHz
R592 1M
12Mhz
S52
S153
SPI-SDI
SPI-SDO
SPI-CS0N
SPI-SCK
R697 1k
3V3_STBY
C571
C572
S180
S181
USB1_DM
USB1_DP
USB2_DM
USB2_DP
KEYBOARD
DVD_SENSE
SC2_PIN8
R825 33R
R824 33R
AGC_SENSE
C66 100n
R425 33R
R826 33R
digital_pen
IR_IN
R35 10k
BACKLIGHT_DIM
R371 4k7
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TS0_SYNC
TS0_CLK
TS_MDO0
TS_MDO1
TS_MDO2
TS_MDO3
TS_MDO4
TS_MDO5
TS_MDO6
TS_MDO7
R581
R582
R584
R585
R583
R589
R587
R586
R588
R577
R578
33R
P_D0
P_D1
P_D2
P_D3
P_D4
P_D5
P_D6
P_D7
P_REG_N
P_RESET
P_WAIT_N
P_CE_N
P_OE_N
P_IRQA_N
P_IOWR_N
P_IORD_N
P_WE_N
P_CD_N
R423 33R
PCM_REG_N
PCM_RST
PCM_WAIT_N
PCM_CE_N
PCM_OE_N
PCM_IRQA_N
PCM_IOWR_N
PCM_IORD_N
PCM_WE_N
PCM_CD_N
TS1VALID
TS1CLK
TS1SYNC
TS1DATA
TSMIVALID
TSMICLK
TSMISYNC
TS_MDI0
C1137 10p 50V
R418 33R
R419 33R
R420 33R
TSMOVALID
TSMOSTART
TSMOCLK
C1138 10p 50V
C1136 10p 50V
CEZ0
0:BOOT FROM NOR FLASH
1:BOOT FROM SPI FLASH
CE1Z
0:8 BIT NOR FLASH
1:10 BIT NOR FLASH
R320 4k7
R319 1k
R318 1k
R342 1k
NC
PF_CE0Z
PF_CE1Z
R382 4k7
R383 4k7
S97
BACKLIGHT_ON/OFF
BACKLIGHT_ON/OFF_M
R381 4k7
Q41 BC848B
C170 100n 10V
R560 47k
R561 47k
R316 1k
R325 1k
IC CONFIGURATION SELECTION
R379 4k7
R332 1k
R333 1k
R331 1k
PCM_OE_N
PCM_WE_N
PCM_IORD_N
PCM_IOWR_N
R2 4k7
R97 4k7
R60 4k7
R6 4k7
S57
S46
VCC_PCMCIA
R1228 4k7
S232
S233
U122 74V1G08
R1245 4k7
R421 33R
C323 10p 50V
C324 10p 50V
S234
R370 4k7
R422 33R
CN6
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PCM_CD2_N
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TSMOSTART
TSMISYNC
R397 4k7
R424 33R
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TS_MDI1
TS_MDI2
TS_MDI3
TS_MDI4
TS_MDI5
TS_MDI6
TS_MDI7
FROM DVB_T
R15 33R
R447 56R
R448 56R
R281 4k7
R391 4k7
R393 4k7
R77 10k
R76 10k
R78 10k
R411 4k7
R412 4k7
Q12 BC848B
Q11 BC848B
5V_VCC
F30 60R
Q158 BSH103
C1135 220u 10V
C1126 220u 10V
C127 330p 50V
C47 100n 16V
C48 100n 16V
C1128 220u 10V
D170 1N4148
12V_VCC
R1221 4k7
R1222 4k7
R1224 33k
R1225 33k
R1227 33k
LED3
PIX2GPIO3
C1120 100n 10V
Q157 BC848B
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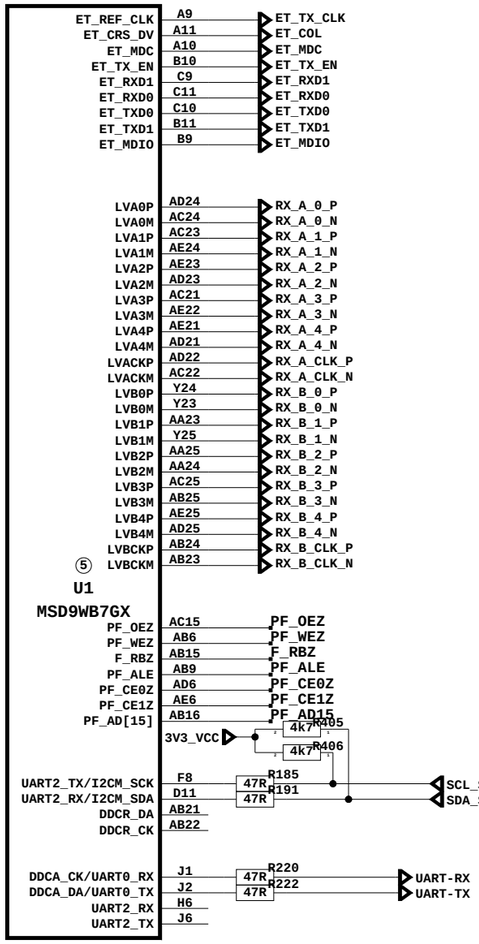
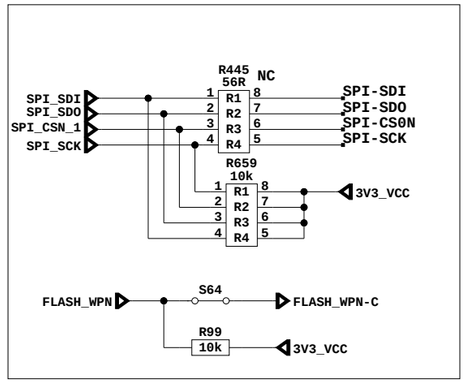
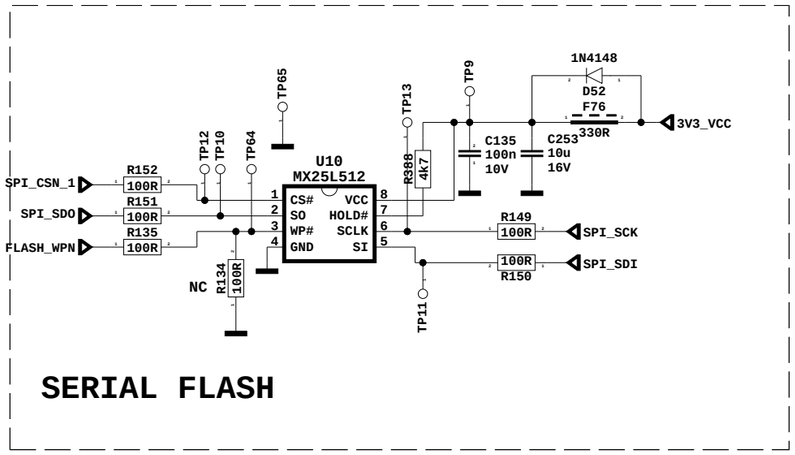
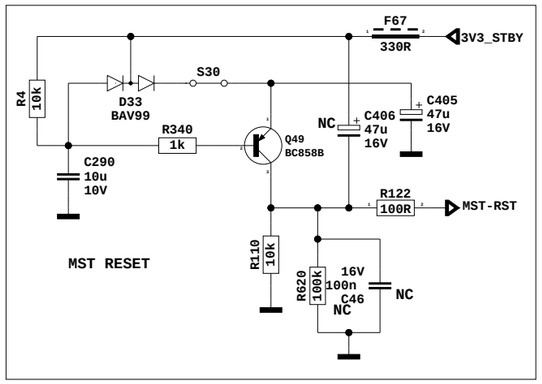
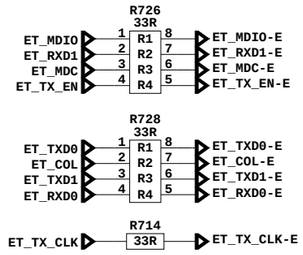
A3
SCH NAME :<DRAWING NAME HERE>
SHEET: 8 OF: 7
DRAWN BY :<YOUR NAME HERE>
12-01-2010_13:26

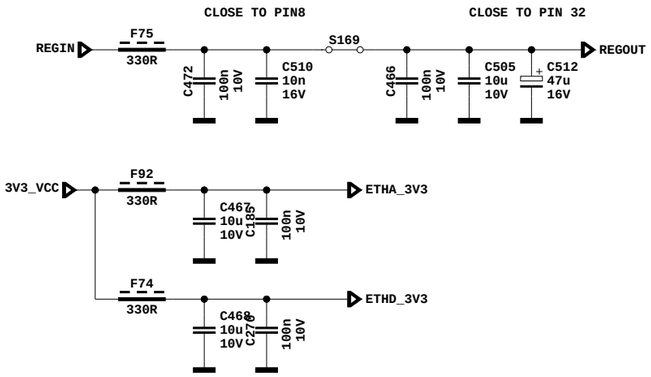


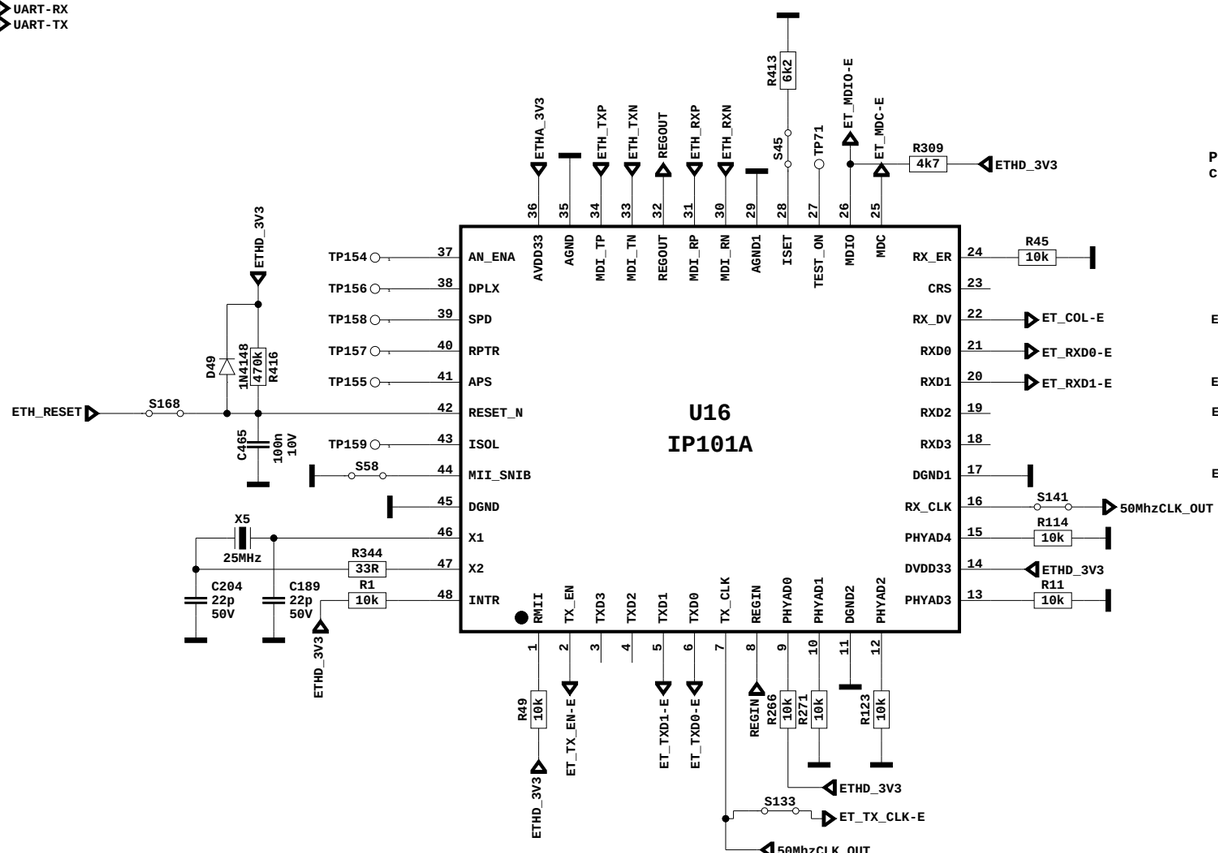


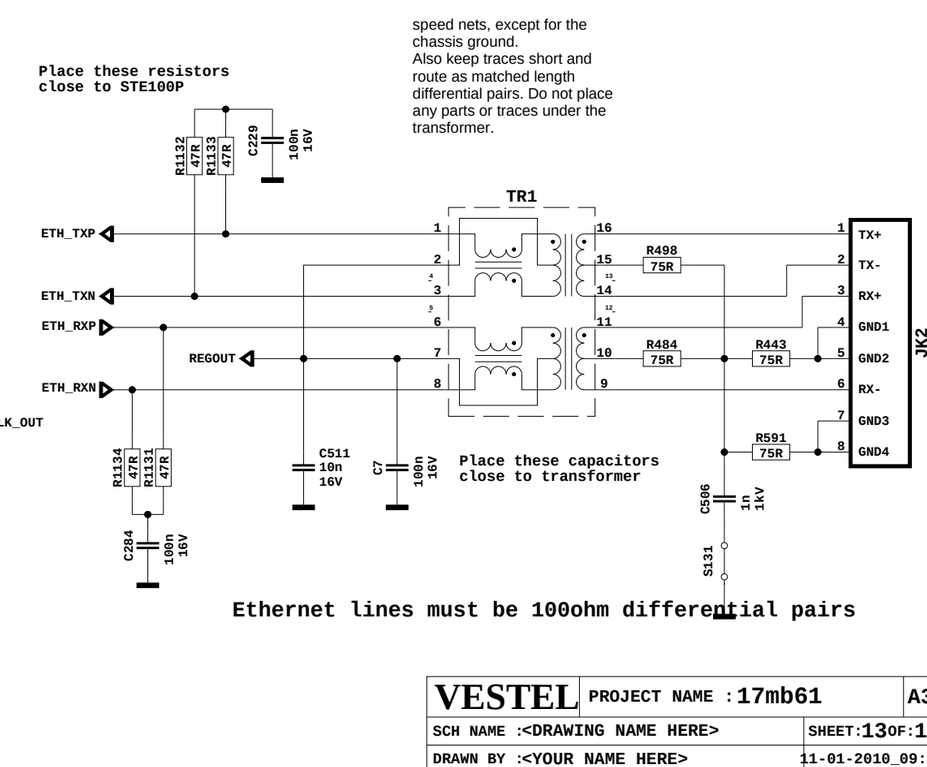












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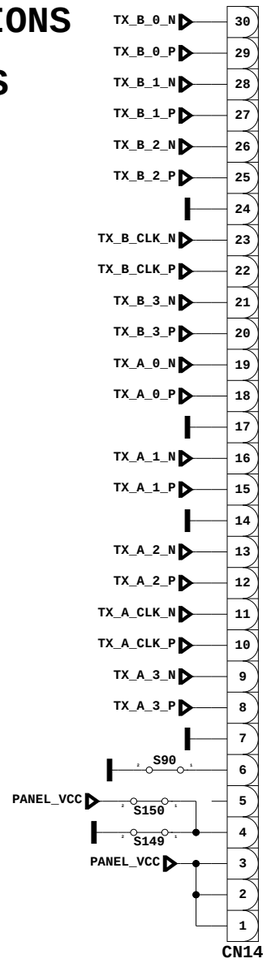
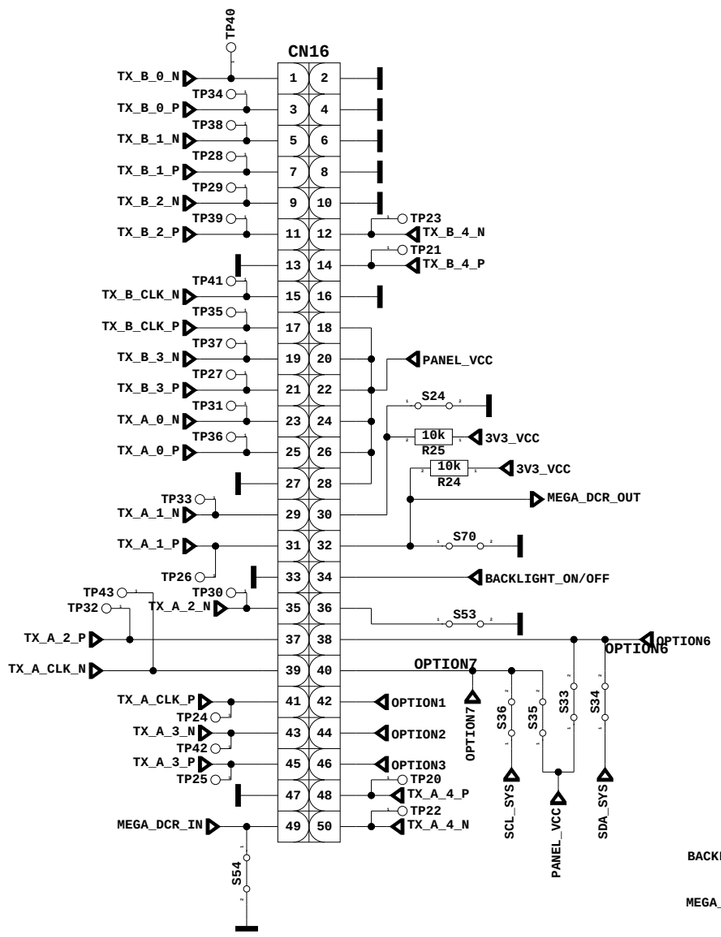
SCH NAME :<DRAWING NAME HERE>		SHEET:13OF:12
DRAWN BY :<YOUR NAME HERE>		11-01-2010_09:27

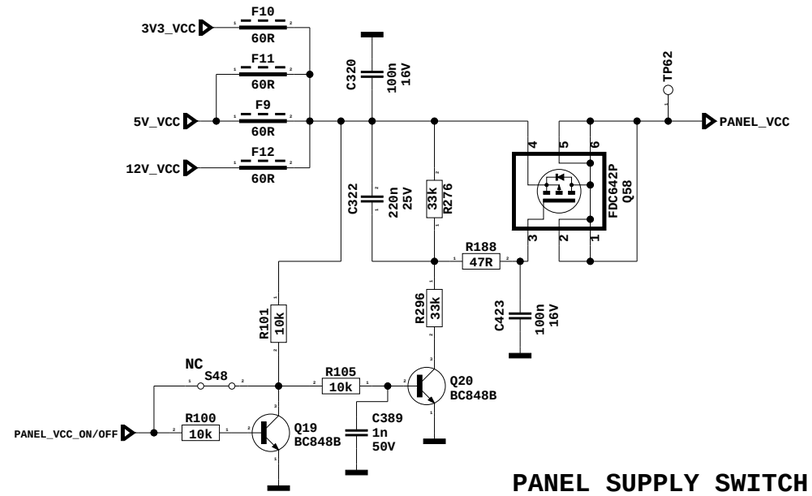
19" TO 22" FFC OPTIONS

26" UT FFC OPTIONS

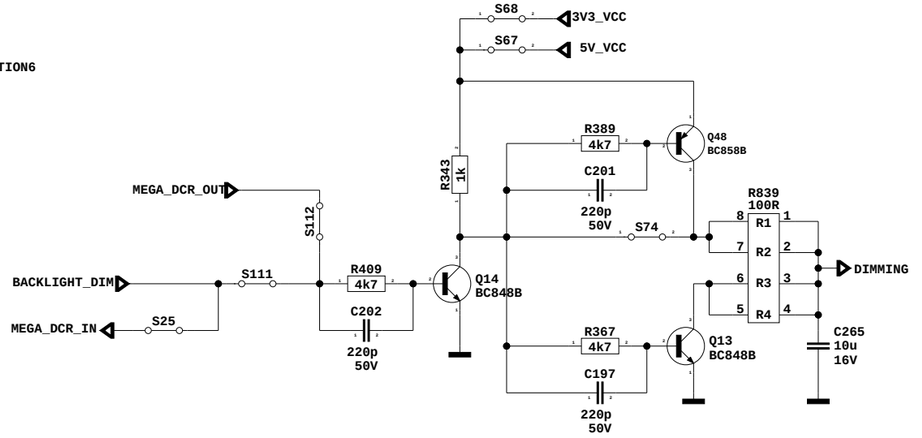


LVDS CABLE

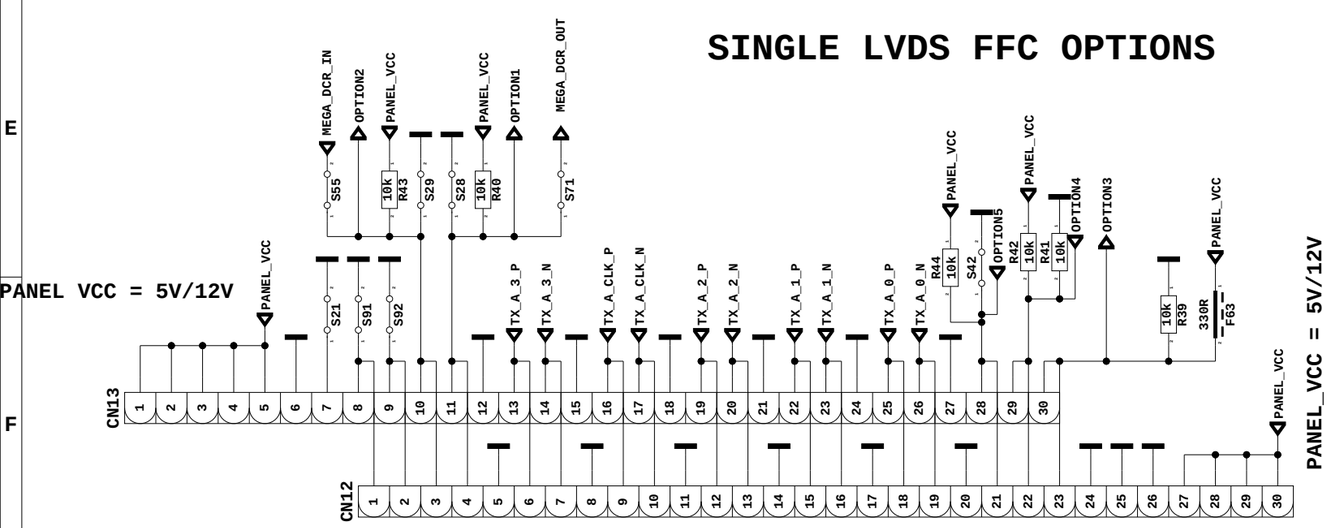


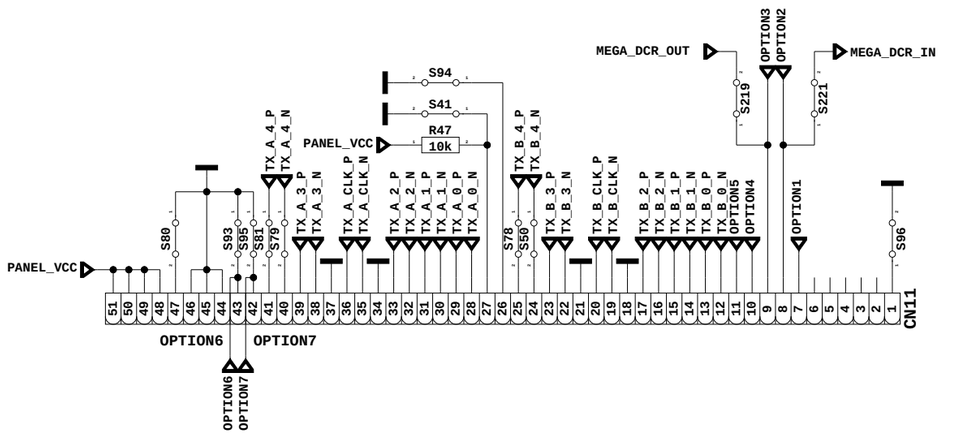


PANEL SUPPLY SWITCH



SINGLE LVDS FFC OPTIONS





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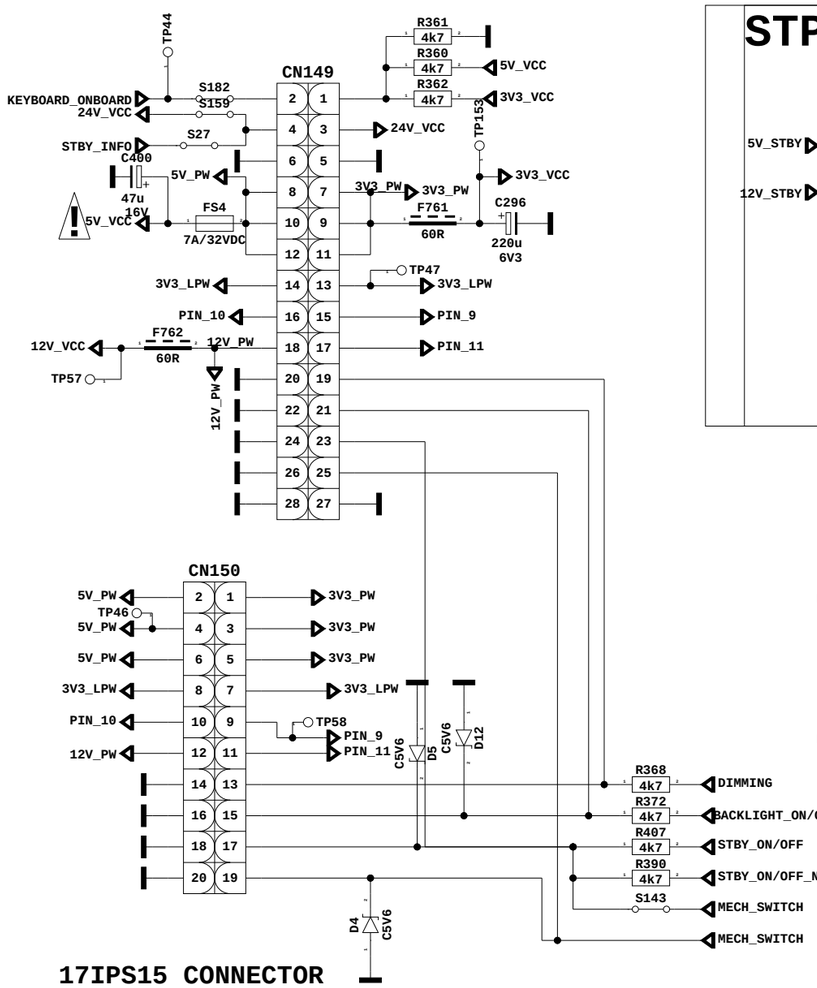
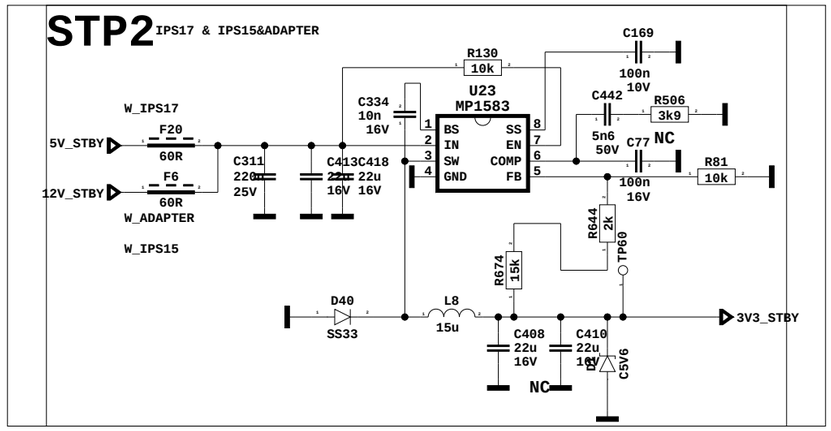
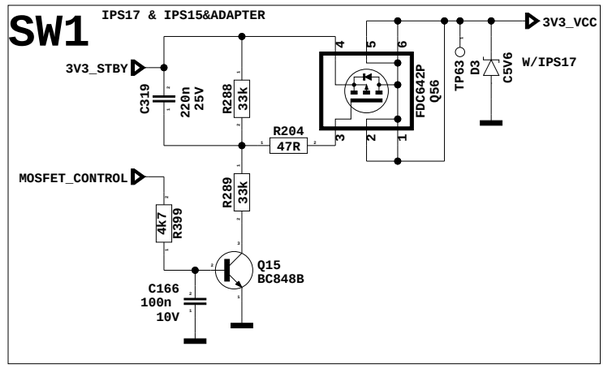
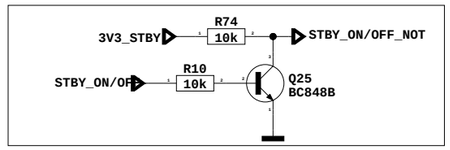
DRAWN BY :<YOUR NAME HERE>	11-01-2010_09:26	

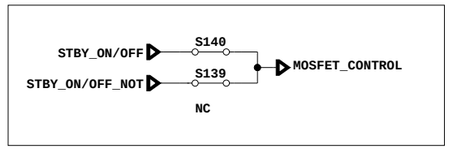


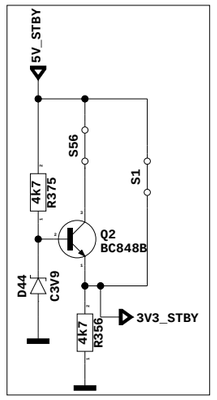
17IPS15 CONNECTOR

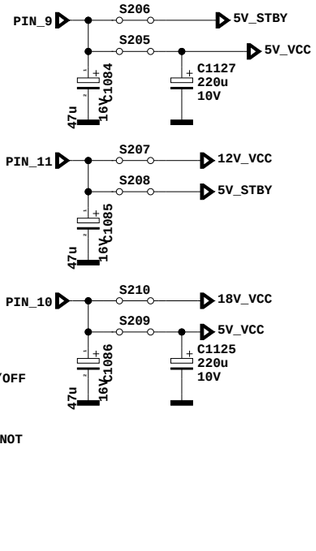


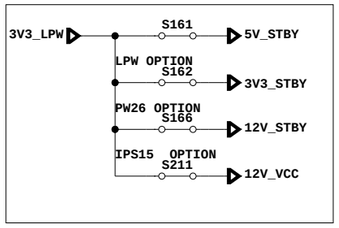


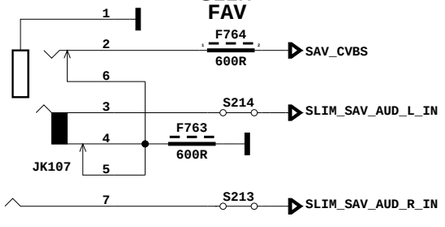


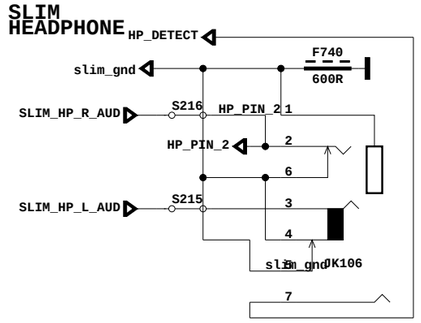


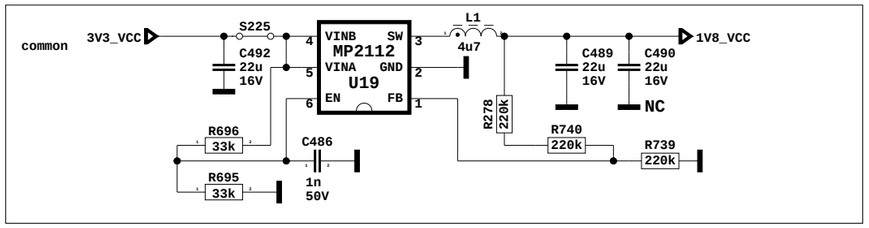


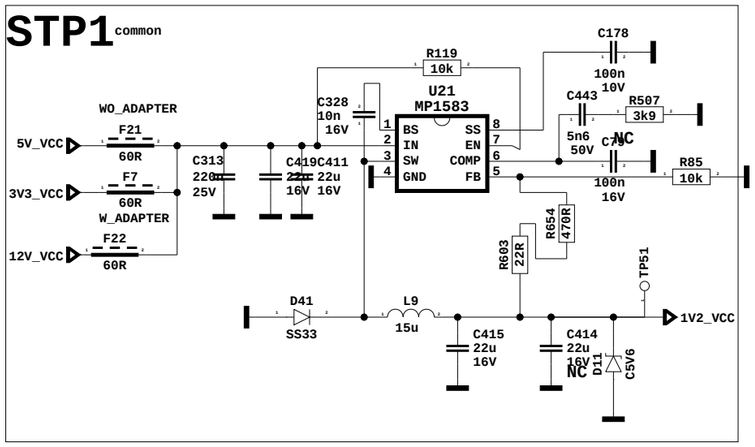


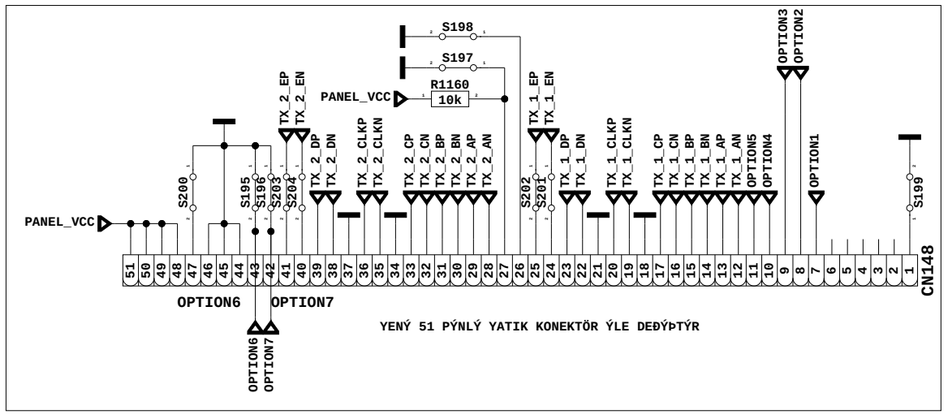












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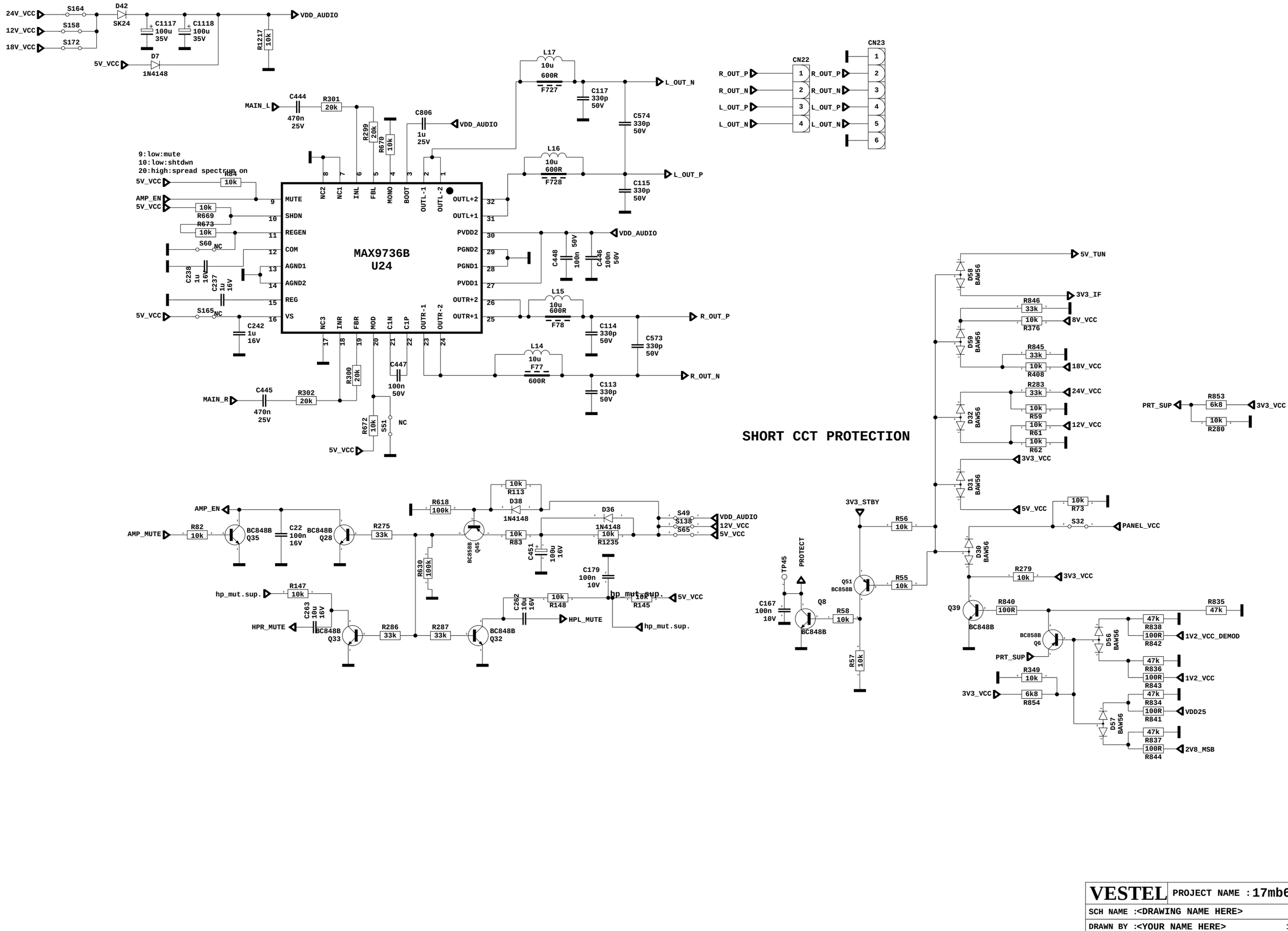

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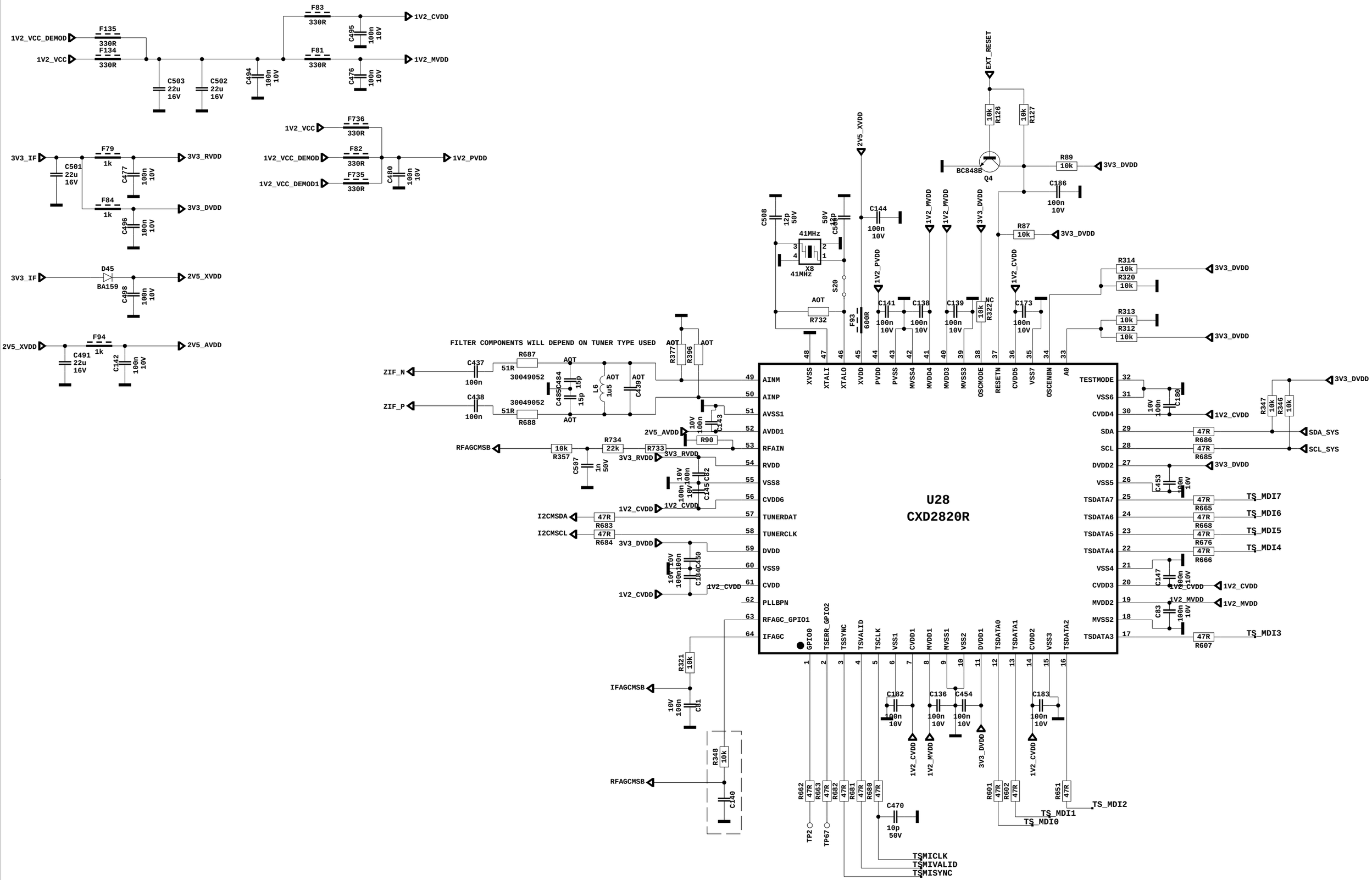
DRAWN BY :<YOUR NAME HERE>	11-01-2010_09:26	



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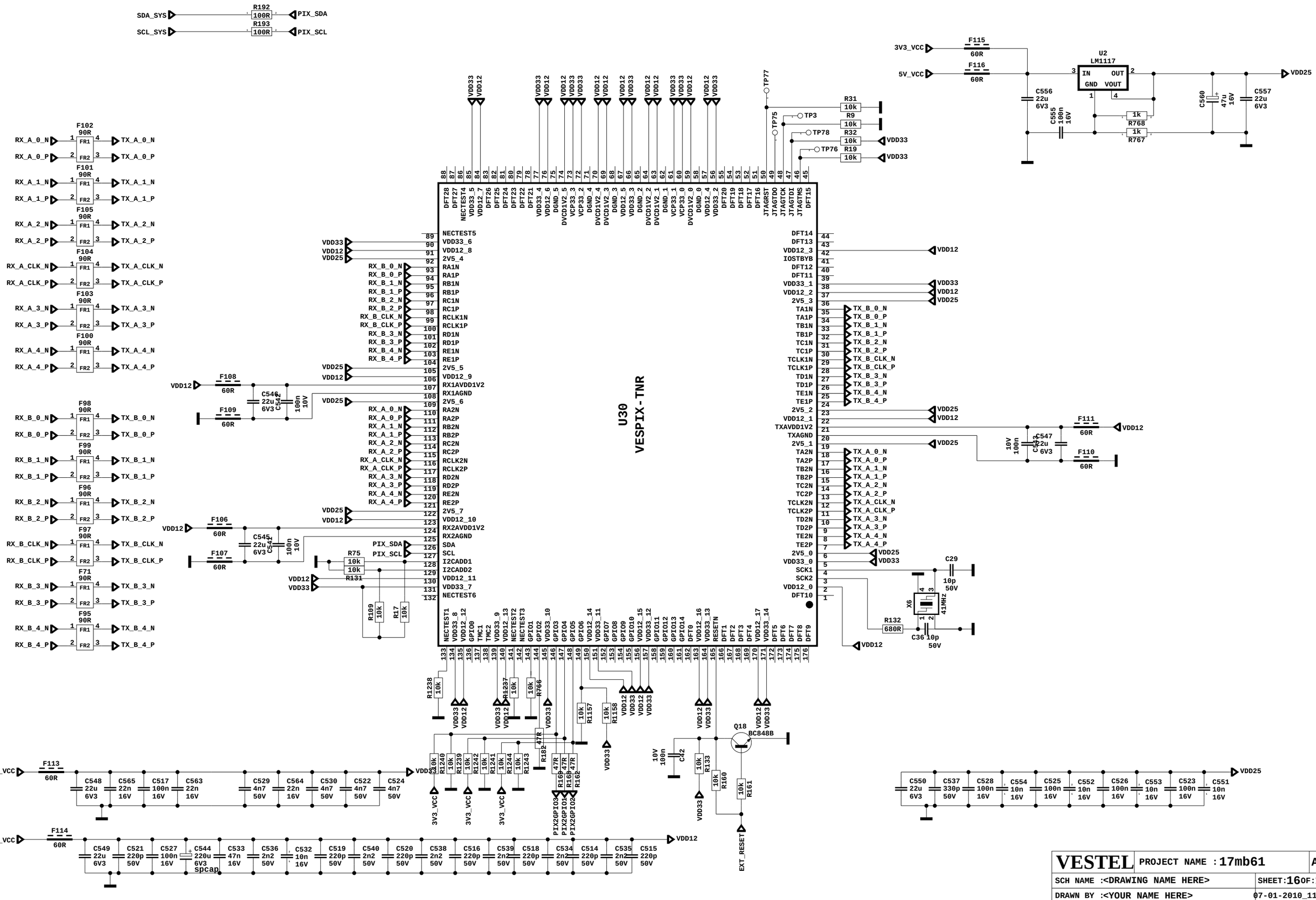
DRAWN BY :<YOUR NAME HERE>		11-01-2010_09:50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SCL_SYS
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PIX_SDA
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F115 60R
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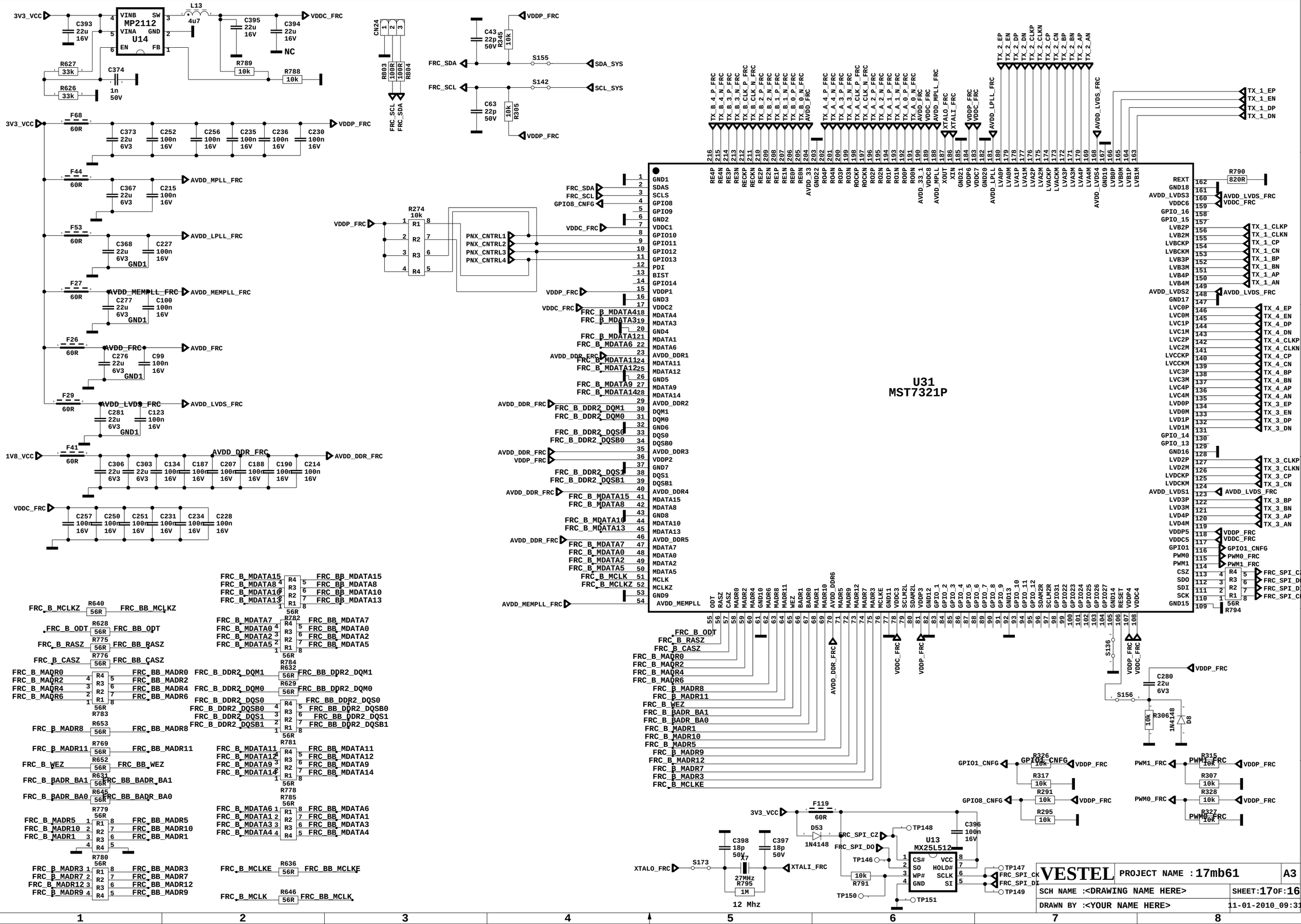
U2 LM1117
IN OUT GND VOUT
VDD25
C556 22u 6V3
C555 100n 16V
C560 47u 16V
C557 22u 6V3
R768 1k
R767 1k
TP77
TP3
TP78
TP76
TP75
R31 10k
R9 10k
R32 10k
R19 10k
VDD33
VDD12
U30
VESPIX-TNR
F102 90R
F101 90R
F105 90R
F104 90R
F103 90R
F100 90R
F98 90R
F99 90R
F96 90R
F97 90R
F71 90R
F95 90R
RX_A_0_N
RX_A_0_P
RX_A_1_N
RX_A_1_P
RX_A_2_N
RX_A_2_P
RX_A_CLK_N
RX_A_CLK_P
RX_A_3_N
RX_A_3_P
RX_A_4_N
RX_A_4_P
RX_B_0_N
RX_B_0_P
RX_B_1_N
RX_B_1_P
RX_B_2_N
RX_B_2_P
RX_B_CLK_N
RX_B_CLK_P
RX_B_3_N
RX_B_3_P
RX_B_4_N
RX_B_4_P
TX_A_0_N
TX_A_0_P
TX_A_1_N
TX_A_1_P
TX_A_2_N
TX_A_2_P
TX_A_CLK_N
TX_A_CLK_P
TX_A_3_N
TX_A_3_P
TX_A_4_N
TX_A_4_P
TX_B_0_N
TX_B_0_P
TX_B_1_N
TX_B_1_P
TX_B_2_N
TX_B_2_P
TX_B_CLK_N
TX_B_CLK_P
TX_B_3_N
TX_B_3_P
TX_B_4_N
TX_B_4_P
F108 60R
F109 60R
F106 60R
F107 60R
C546 22u 6V3
C547 100n 10V
C545 22u 6V3
C544 100n 10V
R75 10k
R131 10k
R109 10k
R17 10k
PIX_SDA
PIX_SCL
F111 60R
F110 60R
C542 22u 6V3
C543 100n 10V
C29 10p 50V
X6 41MHz
C36 10p 50V
R132 680R
Q18 BC848B
C42 10k
R133 10k
R160 10k
R161 10k
EXT_RESET
R182 47R
R1238 10k
R1237 10k
R766 10k
R1157 10k
R1158 10k
R1240 10k
R1239 10k
R1242 10k
R1241 10k
R1244 10k
R1243 10k
R169 47R
R168 47R
R167 47R
R162 47R
PIX2GPIO3
PIX2GPIO1
PIX2GPIO2
F113 60R
F114 60R
3V3_VCC
1V2_VCC
C548 22u 6V3
C565 22n 16V
C517 100n 16V
C563 22n 16V
C529 4n7 50V
C564 22n 16V
C530 4n7 50V
C522 4n7 50V
C524 4n7 50V
C549 22u 6V3
C521 220p 50V
C527 100n 16V
C544 220u 6V3 spcap
C533 47n 16V
C536 2n2 50V
C532 10n 16V
C519 220p 50V
C540 2n2 50V
C520 220p 50V
C538 2n2 50V
C516 220p 50V
C539 2n2 50V
C518 220p 50V
C534 2n2 50V
C514 220p 50V
C535 2n2 50V
C515 220p 50V
C550 22u 6V3
C537 330p 50V
C528 100n 16V
C554 10n 16V
C525 100n 16V
C552 10n 16V
C526 100n 16V
C553 10n 16V
C523 100n 16V
C551 10n 16V
VESTEL
PROJECT NAME :17mb61
A3
SCH NAME :<DRAWING NAME HERE>
SHEET:16OF:15
DRAWN BY :<YOUR NAME HERE>
07-01-2010_11:20


MP2112
U14
VINB SW
VINA GND
EN FB
L13
4u7
C393 22u 16V
C395 22u 16V
C394 22u 16V
NC
R627 33k
R626 33k
C374 1n 50V
R789 10k
R788 10k
3V3_VCC
VDDC_FRC
CN24
R803 100R
R804 100R
FRC_SCL
FRC_SDA
C43 22p 50V
R345 10k
S155
SDA_SYS
S142
SCL_SYS
C63 22p 50V
R305 10k
VDDP_FRC
F68 60R
C373 22u 6V3
C252 100n 16V
C256 100n 16V
C235 100n 16V
C236 100n 16V
C230 100n 16V
F44 60R
C367 22u 6V3
C215 100n 16V
AVDD_MPLL_FRC
F53 60R
C368 22u 6V3
C227 100n 16V
AVDD_LPLL_FRC
GND1
F27 60R
C277 22u 6V3
C100 100n 16V
AVDD_MEMPLL_FRC
F26 60R
C276 22u 6V3
C99 100n 16V
AVDD_FRC
F29 60R
C281 22u 6V3
C123 100n 16V
AVDD_LVDS_FRC
F41 60R
1V8_VCC
C306 22u 6V3
C303 22u 6V3
C134 100n 16V
C187 100n 16V
C207 100n 16V
C188 100n 16V
C190 100n 16V
C214 100n 16V
AVDD_DDR_FRC
C257 100n 16V
C250 100n 16V
C251 100n 16V
C231 100n 16V
C234 100n 16V
C228 100n 16V
R274 10k
PNX_CNTRL1
PNX_CNTRL2
PNX_CNTRL3
PNX_CNTRL4
U31
MST7321P
TX_B_4_P_FRC
TX_B_4_N_FRC
TX_B_3_P_FRC
TX_B_3_N_FRC
TX_B_CLK_P_FRC
TX_B_CLK_N_FRC
TX_B_2_P_FRC
TX_B_2_N_FRC
TX_B_1_P_FRC
TX_B_1_N_FRC
TX_B_0_P_FRC
TX_B_0_N_FRC
AVDD_FRC
TX_A_4_P_FRC
TX_A_4_N_FRC
TX_A_3_P_FRC
TX_A_3_N_FRC
TX_A_CLK_P_FRC
TX_A_CLK_N_FRC
TX_A_2_P_FRC
TX_A_2_N_FRC
TX_A_1_P_FRC
TX_A_1_N_FRC
TX_A_0_P_FRC
TX_A_0_N_FRC
AVDD_FRC
VDDC_FRC
AVDD_MPLL_FRC
XTALO_FRC
XTALI_FRC
VDDP_FRC
VDDC_FRC
AVDD_LPLL_FRC
TX_2_EP
TX_2_EN
TX_2_DP
TX_2_DN
TX_2_CLKP
TX_2_CLKN
TX_2_CP
TX_2_CN
TX_2_BP
TX_2_BN
TX_2_AP
TX_2_AN
AVDD_LVDS_FRC
TX_1_EP
TX_1_EN
TX_1_DP
TX_1_DN
R790 820R
AVDD_LVDS_FRC
VDDC_FRC
TX_1_CLKP
TX_1_CLKN
TX_1_CP
TX_1_CN
TX_1_BP
TX_1_BN
TX_1_AP
TX_1_AN
TX_4_EP
TX_4_EN
TX_4_DP
TX_4_DN
TX_4_CLKP
TX_4_CLKN
TX_4_CP
TX_4_CN
TX_4_BP
TX_4_BN
TX_4_AP
TX_4_AN
TX_3_EP
TX_3_EN
TX_3_DP
TX_3_DN
TX_3_CLKP
TX_3_CLKN
TX_3_CP
TX_3_CN
TX_3_BP
TX_3_BN
TX_3_AP
TX_3_AN
VDDP_FRC
VDDC_FRC
GPIO1_CNFG
PWM0_FRC
PWM1_FRC
FRC_SPI_CZ
FRC_SPI_DO
FRC_SPI_DI
FRC_SPI_CK
FRC_B_MDATA15
FRC_B_MDATA8
FRC_B_MDATA10
FRC_B_MDATA13
FRC_B_MDATA7
FRC_B_MDATA0
FRC_B_MDATA2
FRC_B_MDATA5
FRC_B_MDATA11
FRC_B_MDATA12
FRC_B_MDATA9
FRC_B_MDATA14
FRC_B_MDATA6
FRC_B_MDATA1
FRC_B_MDATA3
FRC_B_MDATA4
FRC_BB_MDATA15
FRC_BB_MDATA8
FRC_BB_MDATA10
FRC_BB_MDATA13
FRC_BB_MDATA7
FRC_BB_MDATA0
FRC_BB_MDATA2
FRC_BB_MDATA5
FRC_BB_MDATA11
FRC_BB_MDATA12
FRC_BB_MDATA9
FRC_BB_MDATA14
FRC_BB_MDATA6
FRC_BB_MDATA1
FRC_BB_MDATA3
FRC_BB_MDATA4
R640 56R
FRC_B_MCLKZ
FRC_BB_MCLKZ
R628 56R
FRC_B_ODT
FRC_BB_ODT
R775 56R
FRC_B_RASZ
FRC_BB_RASZ
R776 56R
FRC_B_CASZ
FRC_BB_CASZ
R782 56R
R784 56R
R632 56R
FRC_B_DDR2_DQM1
FRC_BB_DDR2_DQM1
R629 56R
FRC_B_DDR2_DQM0
FRC_BB_DDR2_DQM0
R633 56R
FRC_B_DDR2_DQS0
FRC_B_DDR2_DQSB0
FRC_B_DDR2_DQS1
FRC_B_DDR2_DQSB1
FRC_BB_DDR2_DQS0
FRC_BB_DDR2_DQSB0
FRC_BB_DDR2_DQS1
FRC_BB_DDR2_DQSB1
R781 56R
R778 56R
R785 56R
R779 56R
R780 56R
R783 56R
R653 56R
FRC_B_MADR8
FRC_BB_MADR8
R769 56R
FRC_B_MADR11
FRC_BB_MADR11
R652 56R
FRC_B_WEZ
FRC_BB_WEZ
R631 56R
FRC_B_BADR_BA1
FRC_BB_BADR_BA1
R645 56R
FRC_B_BADR_BA0
FRC_BB_BADR_BA0
FRC_B_MADR0
FRC_B_MADR2
FRC_B_MADR4
FRC_B_MADR6
FRC_BB_MADR0
FRC_BB_MADR2
FRC_BB_MADR4
FRC_BB_MADR6
FRC_B_MADR5
FRC_B_MADR10
FRC_B_MADR1
FRC_BB_MADR5
FRC_BB_MADR10
FRC_BB_MADR1
FRC_B_MADR3
FRC_B_MADR7
FRC_B_MADR12
FRC_B_MADR9
FRC_BB_MADR3
FRC_BB_MADR7
FRC_BB_MADR12
FRC_BB_MADR9
R636 56R
FRC_B_MCLKE
FRC_BB_MCLKE
R646 56R
FRC_B_MCLK
FRC_BB_MCLK
GND1 GND2 VDDC1 GPIO10 GPIO11 GPIO12 GPIO13 PDI BIST GPIO14 VDDP1 GND3 VDDC2 MDATA4 MDATA3 GND4 MDATA1 MDATA6 AVDD_DDR1 MDATA11 MDATA12 GND5 MDATA9 MDATA14 AVDD_DDR2 DQM1 DQM0 GND6 DQS0 DQSB0 AVDD_DDR3 VDDP2 GND7 DQS1 DQSB1 AVDD_DDR4 MDATA15 MDATA8 GND8 MDATA10 MDATA13 AVDD_DDR5 MDATA7 MDATA0 MDATA2 MDATA5 MCLK MCLKZ GND9 AVDD_MEMPLL
ODT RASZ CASZ MADR0 MADR2 MADR4 GND10 MADR6 MADR8 MADR11 WEZ BADR1 BADR0 MADR1 MADR10 AVDD_DDR_FRC MADR5 MADR9 MADR12 MADR7 MADR3 MCLKE GND11 VDDC3 SCLM2L SDAM2L VDDP3 GND12 GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7 GPIO_8 GPIO_9 GND13 GPIO_10 GPIO_11 GPIO_12 SDAM2R SCLM2R GPIO31 GPIO22 GPIO23 GPIO24 GPIO25 GPIO26 GPIO27 GND14 RESET VDDP4 VDDC4
REXT GND18 AVDD_LVDS3 VDDC6 GPIO_16 GPIO_15 LVB2P LVB2M LVBCKP LVBCKM LVB3P LVB3M LVB4P LVB4M AVDD_LVDS2 GND17 LVC0P LVC0M LVC1P LVC1M LVC2P LVC2M LVCCKP LVCCKM LVC3P LVC3M LVC4P LVC4M VDDP LVD0M LVD1P LVD1M GPIO_14 GPIO_13 GND16 LVD2P LVD2M LVDCKP LVDCKM AVDD_LVDS1 LVD3P LVD3M LVD4P LVD4M VDDP5 VDDC5 GPIO1 PWM0 PWM1 CSZ SDO SDI SCK GND15
R794 56R
S136
S156
C280 22u 6V3
R306 10k
D8 1N4148
R326 10k
R317 10k
R291 10k
R295 10k
R315 10k
R307 10k
R328 10k
R327 10k
F119 60R
D53 1N4148
C398 18p 50V
C397 18p 50V
X7 27MHz
R795 1M
12 Mhz
S173
XTALO_FRC
XTALI_FRC
U13
MX25L512
CS# SO WP# GND VCC HOLD# SCLK SI
C396 100n 16V
R791 10k
TP146
TP147
TP148
TP149
TP150
TP151
VESTEL
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A3
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SHEET:17OF:16
DRAWN BY :<YOUR NAME HERE>
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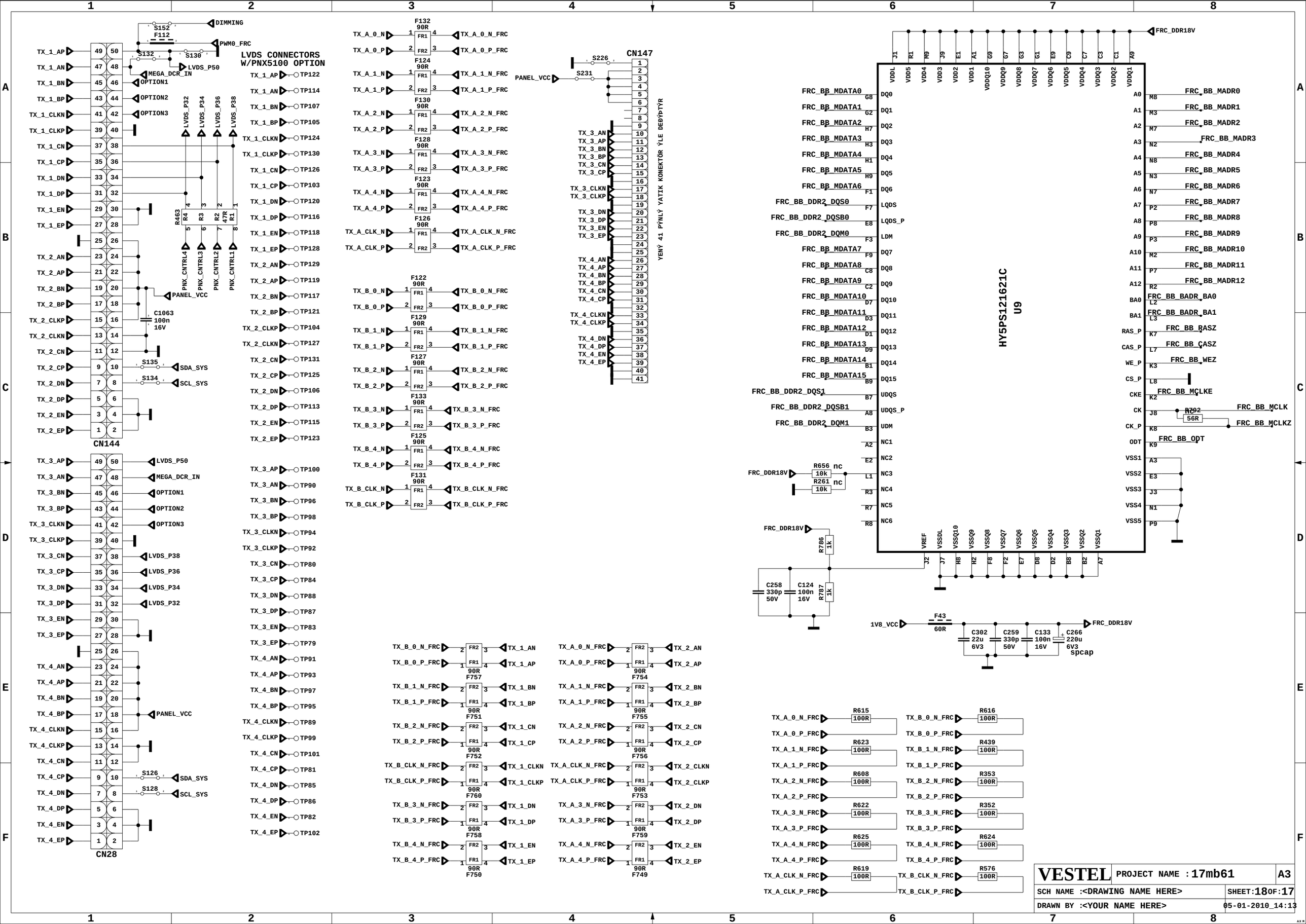
CN144
CN28
LVDS CONNECTORS
W/PNX5100 OPTION
DIMMING
PWM0_FRC
LVDS_P50
MEGA_DCR_IN
OPTION1
OPTION2
OPTION3
PANEL_VCC
SDA_SYS
SCL_SYS
CN147
S226
S231
PANEL_VCC
YENÝ 41 PÝNLÝ YATIK KONEKTÖR ÝLE DEDÝÞTÝR
HY5PS121621C
U9
FRC_DDR18V
1V8_VCC
R656 nc
R261 nc
R786 1k
R787 1k
C258 330p 50V
C124 100n 16V
F43 60R
C302 22u 6V3
C259 330p 50V
C133 100n 16V
C266 220u 6V3
spcap
R792 56R
C1063 100n 16V
VESTEL
PROJECT NAME :17mb61
A3
SCH NAME :<DRAWING NAME HERE>
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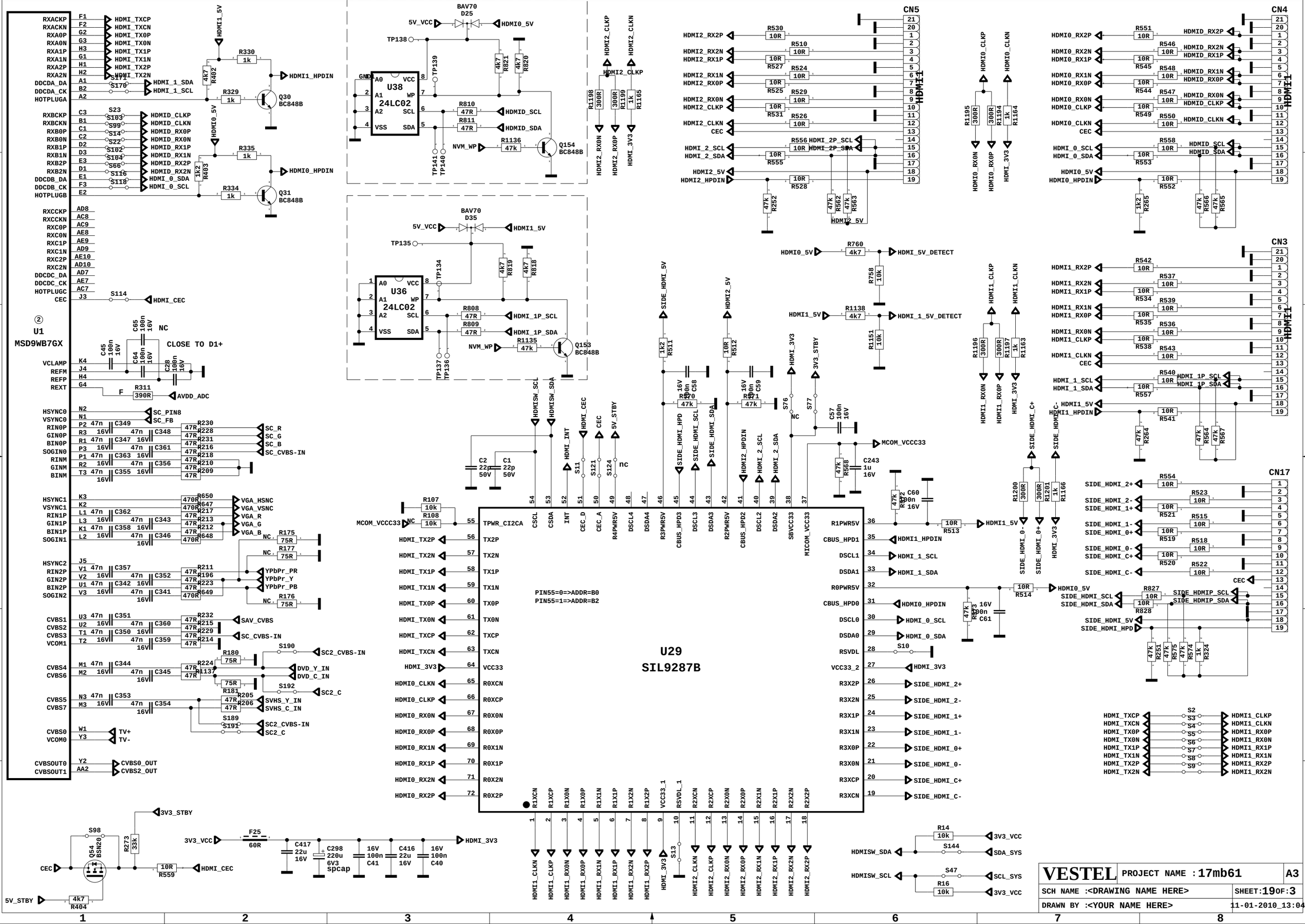
U1
MSD9WB7GX
U38
24LC02
U36
24LC02
U29
SIL9287B
CN5
CN4
CN3
CN17
HDMI1_5V
HDMI0_5V
HDMI2_5V
HDMI1_HPDIN
HDMI0_HPDIN
HDMI2_HPDIN
HDMI_1_SDA
HDMI_1_SCL
HDMI_0_SDA
HDMI_0_SCL
HDMI_CEC
VGA_HSNC
VGA_VSNC
VGA_R
VGA_G
VGA_B
YPbPr_PR
YPbPr_Y
YPbPr_PB
SAV_CVBS
SC_CVBS-IN
SC2_CVBS-IN
DVD_Y_IN
DVD_C_IN
SC2_C
SVHS_Y_IN
SVHS_C_IN
TV+
TV-
CVBS0_OUT
CVBS2_OUT
SC_R
SC_G
SC_B
SC_CVBS-IN
HDMI_5V_DETECT
HDMI_1_5V_DETECT
MCOM_VCCC33
HDMI1_5V
HDMI_3V3
3V3_STBY
3V3_VCC
SDA_SYS
SCL_SYS
PROJECT NAME :17mb61
A3
SCH NAME :<DRAWING NAME HERE>
SHEET:19OF:3
DRAWN BY :<YOUR NAME HERE>
11-01-2010_13:04

SCART1 VIDEO OUTPUT AMPLIFIER

INDIA OPTION

SCART2 VIDEO OUTPUT AMPLIFIER

INDIA OPTION

HEADPHONE

YPBPR INPUT

SIDE AV INPUT

VESTEL	PROJECT NAME : 17mb61	A3
SCH NAME :<DRAWING NAME HERE>	SHEET:20 OF:2	
DRAWN BY :<YOUR NAME HERE>	12-01-2010_17:09