MB45 IDTV
SERVICE MANUAL

1 INTRODUCTION

17MB45-2 mainboard is based on MSTAR concept IC. This IC is capable of handling audio processing, video processing, scaling-display processing, 2D comb filter, OSD and text processing, 8 bit dual LVDS transmitter.

TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo.

Sound system is able to supply 2x2.5W (10%THD) audio output power for stereo speakers.
Supported peripherals are:

The analog part of the moard can support DVD module which is connected to mainboard through a cable.
The USB feature is supported through digital part of the mainboard.

1 RF input VHF1, VHF3, UHF @ 75Ohm(Common)
1 Side AV (CVBS, R/L_Audio) (Common)
1 SCART socket(Common)
1 PC input(Common)
1 Headphone(Optional)
1 Common interface(Optional)
1 Digital USB(Optional)
1 HDMI (Optional)

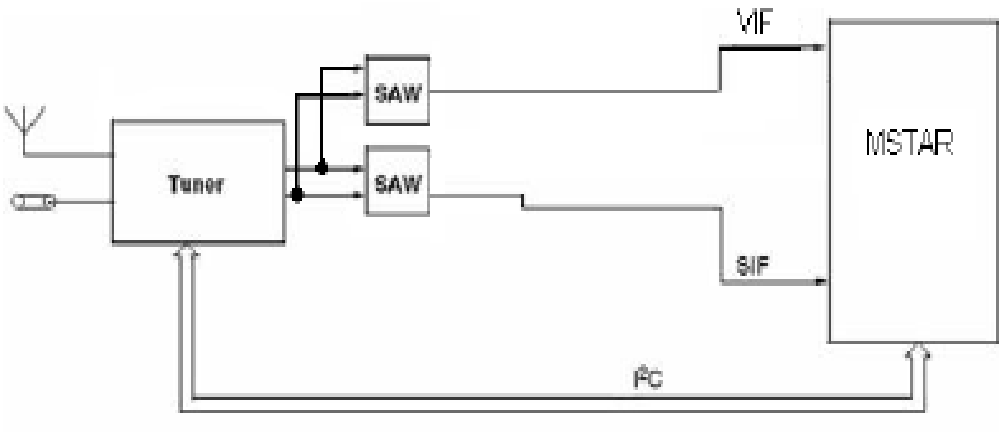
2 TUNER

A horizontal mounted and Digital Half-Nim tuner is used in the product, which covers 3 Bands(From 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on the Tuner in use.

2.1 General description of TDTC-G101D:

The Tuner covers 3 Bands(from 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). Band selection and Tuning are performed digitally via the I2C bus.

Tuner and Main IC connections for analog:



2.2 Features of TDTC-G101D:

- Digital Half-NIM tuner for COFDM
- Covers 3 Bands(From 48MHz to 862MHz for COFDM,
- From 45.25MHz to 863.25MHz for CCIR CH)
- Including IF AGC with SAW Filter
- Bandwidth Switching (7/8 MHz) possible
- DC/DC Converter built in for Tuning Voltage
- Internal(or External) RF AGC, Antenna Power Optional

2.3 Pin Configuration:

PIN NAME	PIN No.	PIN Description
Ant PWR	1	+5V (for Active Antenna), Optional
B1	2	+ 5V (for Loop through & DC-DC)
RF AGC	3	N.C
SCL	4	I²C Bus for TUNER PLL
SDA	5	I²C Bus for TUNER PLL
B2	6	+ 5V (for TU & IF AGC AMP)
Vtu T.P	7	N.C
AS	8	PLL IC Address selection
IF AGC Control	9	IF AGC Control
DIF2	10	Total IF Output2
DIF1	11	Total IF Output1
AIF	12	Tuner IF Output

3 SAW FILTER

3.1 IF Filter for Audio Applications – Epcos K9656M

3.1.1 Standarts

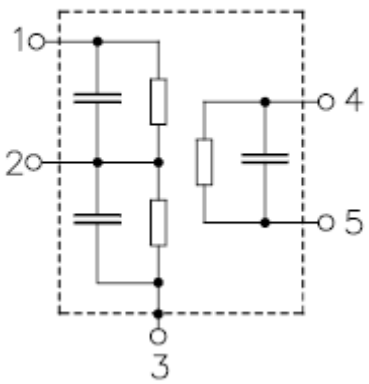
- B/G
- D/K
- I
- L/L'

3.1.2 Features

- TV IF audio filter with two channels
- Channel 1 (L') with one pass band for sound carriers at 40,40 MHz (L') and 39,75 MHz (L'- NICAM)
- Channel 2 (B/G,D/K,L,I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

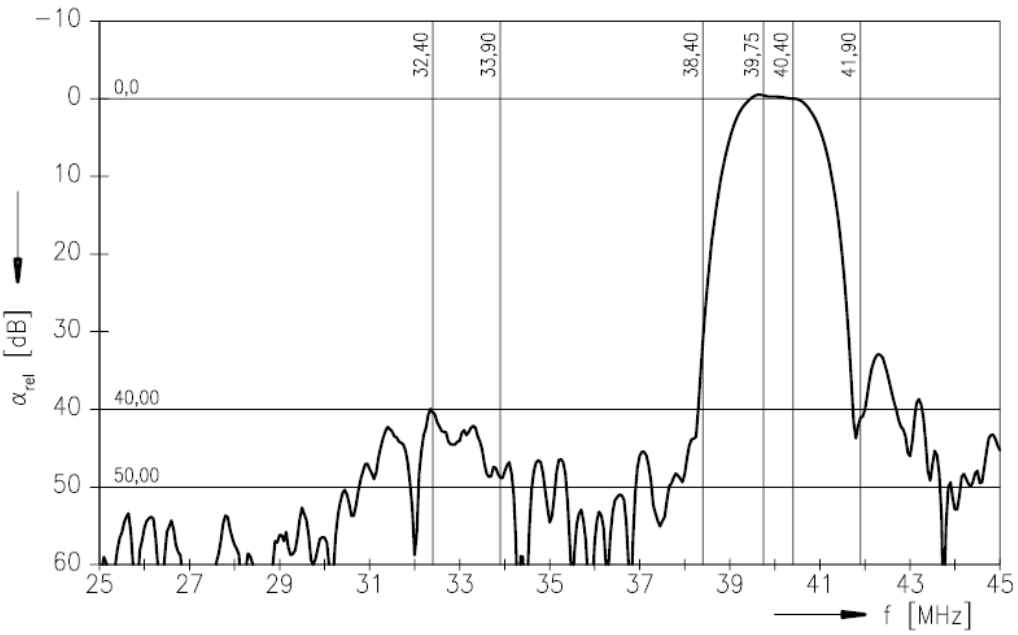
3.1.3 Pin Configuration

1 Input
2 Switching input
3 Chip carrier - ground
4 Output
5 Output

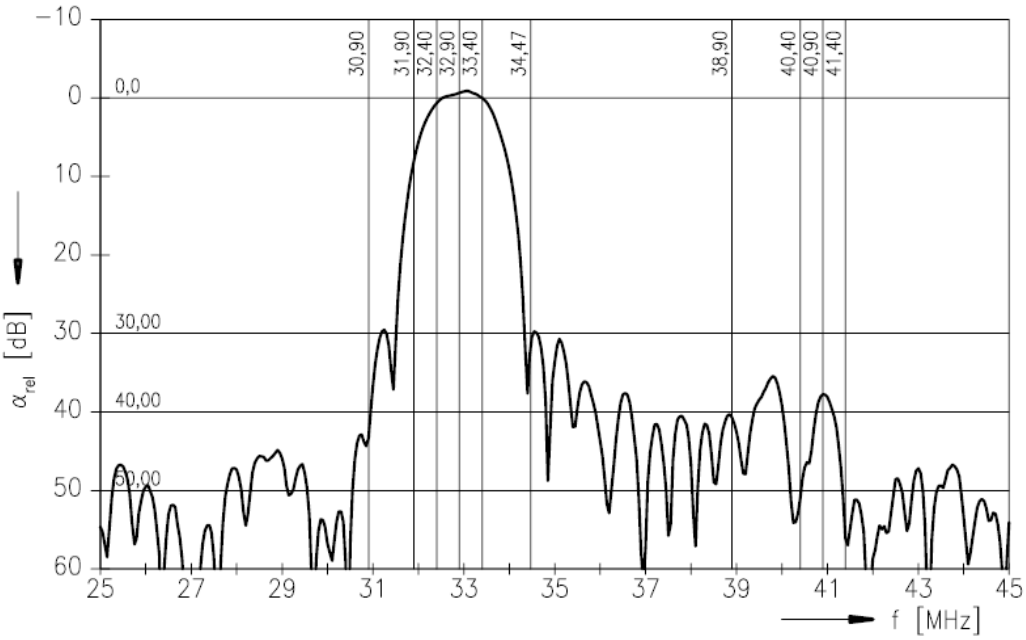


3.1.4 Frequency Response

Frequency Response of Channel 1:



Frequency Response of Channel 2:



3.2 IF Filter for Video Applications – Epcos K3958M

3.2.1 Standarts

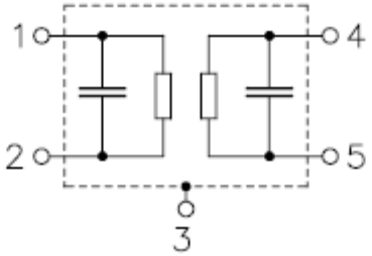
- B/G
- D/K
- I
- L/L'

3.2.2 Features

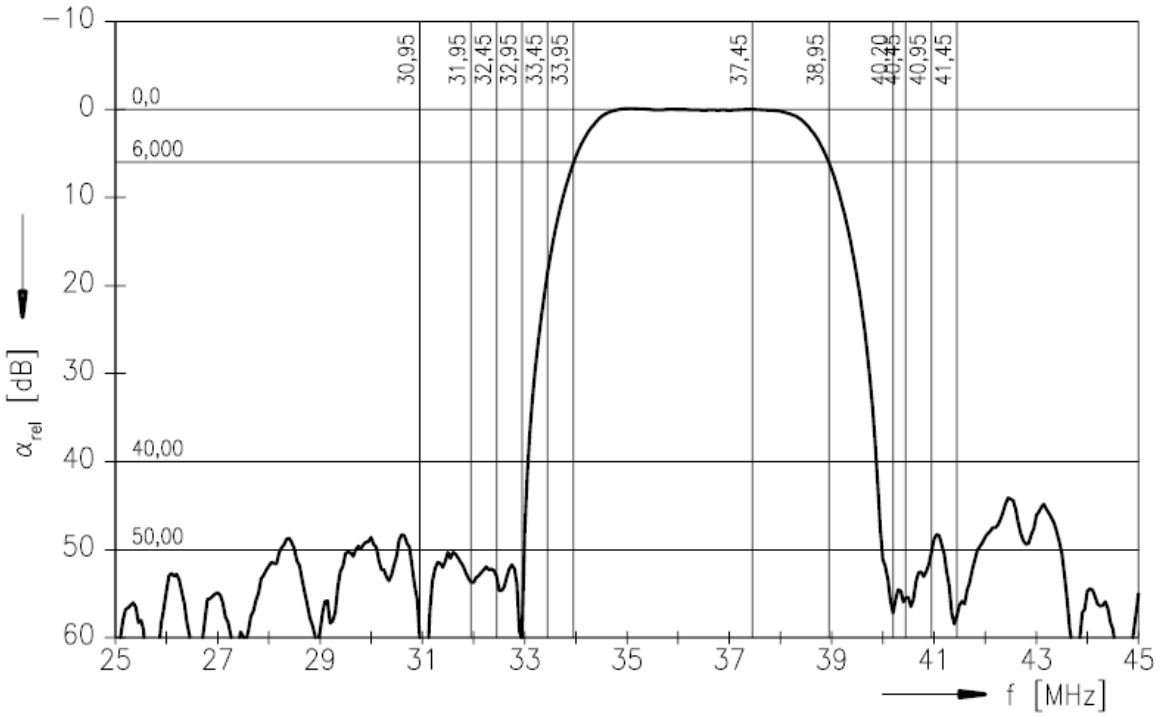
- TV IF filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

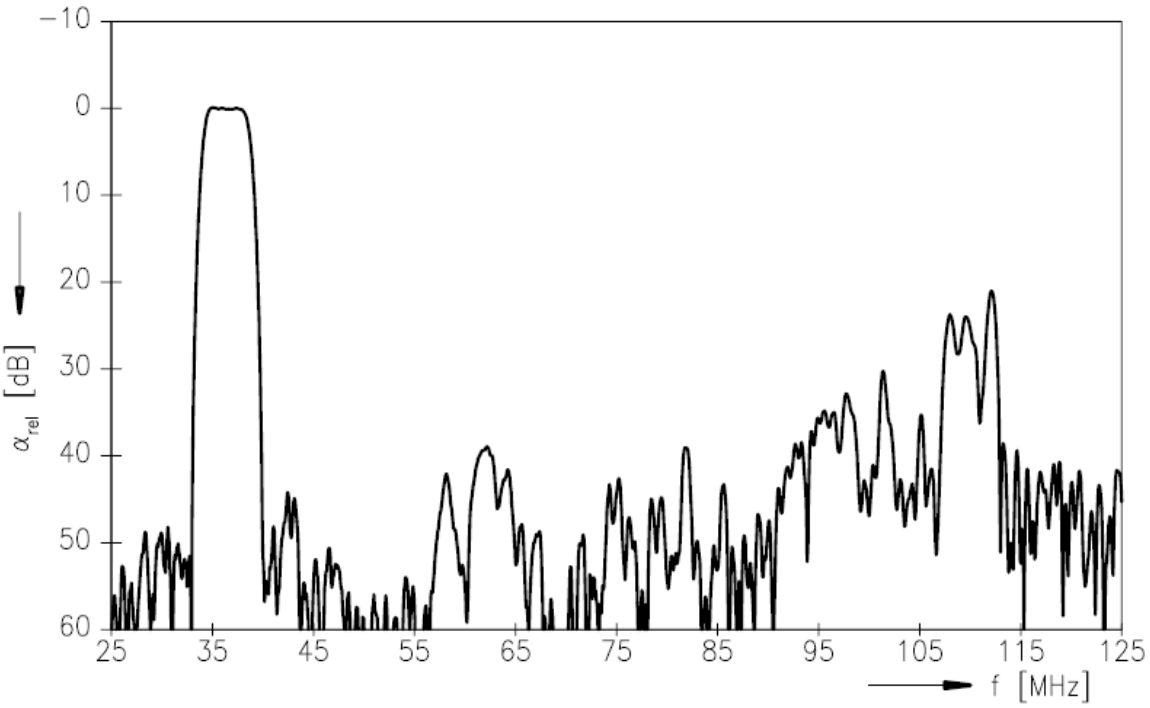
3.2.3 Pin Configuration

1 Input
2 Input - ground
3 Chip - carrier ground
4 Output
5 Output



3.2.4 Frequency Response





4 AUDIO AMPLIFIER STAGE WITH PT2333

4.1 General Description of PT2333:

The PT2333 is a Class-D power amplifier designed for audio equipments, maximum output power can reach up to 2.5W (VDD=5V, RL=4Ω, THD=10%). The PT2333 composed of exclusively designed Class-D circuitry (patented) by PTC, along with the most advanced semi-conductor technology. When compared to the traditional Class-AB amplifiers, the PT2333's has a much higher efficiency (>80%), low heat dissipation, and produces superior audio quality. PT2333's external circuitry is simple and easily accessible, and consists of flawless self-protection capabilities. The chip's packaging is small, thus it occupies an insignificant amount of space on the circuit board; therefore, making it the predominant choice when it comes to audio amplifiers.

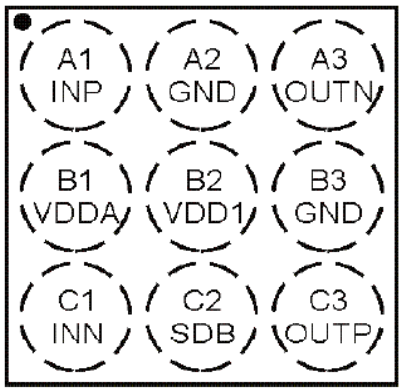
4.2 Features of PT2333:

• CMOS technology
• Operating voltage range from 2.7V up to 5.5V
• Differential analog input
• Maximum output power 2.5W(4Ω) @ THD=10%
• Output low-pass LC filter is not required.
• Voltage gain determinate by the external resister
• Contains shutdown function
• POP noises free in shutdown and power ON/OFF period
• Built-in short circuit protection
• Built-in overheat protection

• High efficiency (8Ω load >85%), low heat dissipation
• Available in MSOP 10-pin and WLCSP 9-pin miniature packages

4.3 Pin Configuration of PT2333:

WLCSP-9 PACKAGE:



(Top View)

Pin	I/O	Symbol	Description	Pin	I/O	Symbol	Description
A1	I	INP	Positive input	B3	Power	GND	Ground
A2	Power	GND	Ground	C1	I	INN	Negative input
A3	O	OUTN	Negative output	C2	I	SDB	Shutdown input
B1	Power	VDDA	Power input	C3	O	OUTP	Positive output
B2	Power	VDD1	Power input	-	-	-	-

5 MICROCONTROLLER (MSTAR)

5.1 Genaral Description

The MST9WB6JS is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to UXGA (1600*1200)/WSXGA+ (1680*1050). It is configured with an integrated DVI/HDCP/HDMI receiver, a multi standard TV video and audio decoder, a video deinterlacer, a scaling engine, the MSTARACE-3 color engine, an on-screen display controller and a built in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST9WB6JS also integrates intelligent power management control capability for green-mode requirements and spread spectrum support for EMI management.

5.2 Features

- Single display LCD TV controller with PC & multimedia display functions
- Input supports up to UXGA & 1080P
- Panel supports up to UXGA(1600x1200) / WSXGA+(1680x1050)
- TV decoder with comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 2-D video de-interlacers
- 3-D video noise reduction
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controller engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8 bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 216-pin LQFP

■ NTSC/PAL/SECAM Video Decoder
- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- 3-D Comb filter for NTSC/PAL
- 5 configurable CVBS & Y/C S-video inputs
- Supports Closed-caption, and V-chip
- CVBS video output

■ Video IF for Multi-Standard Analog TV
- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

■ Multi-Standard TV Sound Decoding/Processing
- Supports BTSC/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- Support MP3 decode
- Programmable delay for audio/video synchronization
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, and P/G EQ
- Optional advanced surround available (Dolby[1], SRS[2], BBE[3]... etc) Note

■ Digital Audio Interface
- I^2S digital audio input & output
- S/PDIF digital audio output
- HDMI audio channel processing capability
- Audio Line-In L/R x2
- Audio Line-Out L/R x3
- Built-in audio DAC L/R x3
- Built-in audio ADC L/R x1
- SIF audio input

■ Analog RGB Compliant Input Ports
- Two analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

■ DVI/HDCP/HDMI Compliant Input Port
- Two DVI/HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
- High Definition Multimedia Interface (HDMI) 1.3 compliant receiver with CEC support
- Long-cable tolerant robust receiving
- Support HDTV up to 1080P

6 INTEGRATED DVB-T RECEIVER (CHEERTEK)

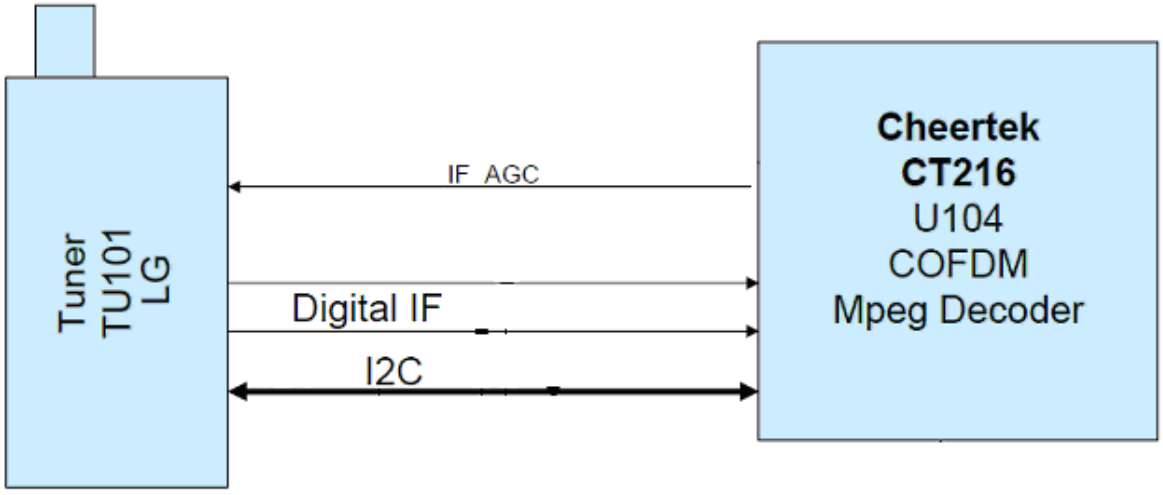
6.1 General Description

CT216T is a highly integrated single chip for DVB-T compliant STB solution. Compared with Cheertek's previous generations of STB receiver devices. CT216T further interates COFDM demodulator USB 2.0 HS host controller, memory card reader, 1/2-bit SPIFlash interface, audio DAC, PWM in/out and SAR-ADC functions. In additiont special enhangements are provided such as MPEG-4 video decoding, 16-bit OSD with anti-flickering, HW JPEG decoding, flesh tone and black-white extensions, and improvement of small video quality.

CT216T includes COFDM demodulator transport stream de-multiplexer, DVB-CSA compliant de-scrambler, RISC MPUs, MPEG-1/2/4 AV decoder, digital TV encoder, audio DACs, USB 2.0 HS host controller, memory card reader, smart card reader, CI controller and other peripherals.

Cli216T is designed in focus on the market of single tuner input product which makes, it a cost effective solution. Supports include free to air, conditional access for SC (Smart card) and CI portable devices, PVR, LCD TV, and other DVB-T applications.

Digital Front End Diagram:



6.2 Features

COFDM Demodulator

- ETSI EN 300 744 DVB-T NorDig Unified 1.0.3, and D-book compliant
- Automatic spectral inversion, detection
- Integrated ADC
- Direct IF (36.167 MHz or 43.75 MHz) or low IF (4.57 MHz) supported
- Single IF AGC or dual RF/lF AGC controls with ΔΣ modulabon
- Impulsive noise cancellation
- Carrier acquisition range: ±400 kHz (extensible to ±600 kHz in 8MHz BW)

- Adjacent channel interference (ACI) filter,for supporting 6, 7, and 8MHz channels with one 8MHz analog filter
- Co-channel interterence (CCl) supression
- RF signal strength monitor

MPU
- Three 32-bit RISC MPU run up to 166MHz with total 448DMIPS
- 8KB I-Cache and 8KB D-Cache
- Two general purpose timers
- Watchdog timer
- DSU for source level debug

Memory
- 6-bit SDRAM controller supports up to 32MB (16MB for l28-pin)
- Unified memory architecture
- Parallel flash (216-pin only)
- 1/2-bit SPI flash

Transport De-multiplexing
- TS, PES, and ES demultiplexing
- OneTS path
- CI CAM interface (216-pin only)
- 32 general purpose PID filters
- 32 Section filters
- CRC-32 accelerator
- DVB-CSA de-scramblers

Video Decoding and Processing
- MPEG-2 MP@ML
- MPEG-4 SP&ASP
- PAL/NTSC format conversion
- 3:2 pull down
- Zoom in/out from 1/16X to 16X
- HW JPEG decode
- 4/8/16-bit OSD with anti-flickering
- On chip NTSC/PAL TV encoder
- CVBS, S-VHS, and component video
- VBI insertion for Teletext, CC and WSS
- ITU-R BT.601 and ITU-R BT.656 outputs
- Flesh tone extension
- Black/white extension,

Audio Decoding and Processing
- MPEG-1: layer 1/2/3
- MPEG-2: layer 1/2
- Decode MPEG-2 and MPEG-1 audio at sampling frequency of 16K, 22.05K, 24K, 32K, 44.1K, and 48KHz
- Decode CU-DA at sampling frequency of 44.1 KHz

- SPDIF out for AC-3 by-pass
- Embedded 2 channels audio DAC for L/R outputs
- Digital mute control and volume adjustment

OSD(On Screen Display)
- There are total 9 display planes: border; background. video. RS1 (Rectangle Strip 1), RS2, OSD, RS3, RS4, and cursor.
- 4/8l16-bit OSD with anti-flickering and anti-flutter
- Support alpha-blending per color
- Adjustable brightness control in window
- Bitmap OSD
- Support horizontal pixel duplication to enlarge bitmap automatically
- Support sub-region redraw to facilitate bitmap display.

Digitnal TV Encoder
- NTSC-M, PAL-B, D, G, H, I, Nc, M encoding
- Four video DACs to provide 6 configuration output: modes
- Support CVBS, S-VHS. and component video outs
- VBI insertion for Teletext, CC and WSS
- Color burst amplitude control
- Programmable sync. level
- On chip, color-bar generator

High Speed I/O
- USB 2.0 HS host controller
- Memory card reader with SD, MMC, and MS interfaces
- Compliant with SD spec. 1.1 and MMC spec. 4.0 with 1-bit & 4-bit modes.
- Compliant with Memory Stick Pro format spec. 1.02 and Memory stick format spec 1.43 with 1-bit and 4-bit modes.

Peripherals
- Up to 3 full duplex UART with 16-byte FIFO
- 2-wire serial (2WS) in master mode .. .
- Up to 2 IS0-7816 compliant SC (1 in 128-pin, can also be used as UART)
- 5 digits 7-Segrnent LED control
- 5x3 two-dimension key scan
- 2 SAR-ADC input
- 4 PWM input/output
- 1 HW IR command decode
- GPIO

Electrical and Physical Characteristics
- Capable of using single 27MHz clock input crystal
- 1.8V and 3.3V dual power supply
- Power standby mode
- PQFP-128 (CT216T-Z) or LQFP-216 (CT216T-R) package

7. 4MX16 BIT SYNCHRONOUS DRAM (DIGITAL SIDE SDRAM)

7.1 General Description

The EM638165 SDRAM is a high-speed CMOS synchronous DRAM containing 64 Mbits. It is internally configured as 4 Banks of 1M word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM638165 provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications.

7.2 Features

- Fast access time from clock: 4.5/5/5.4 ns
- Fast clock rate: 200/166/143 MHz
- Fully synchronous operation
- Internal pipelined architecture
- 1M word x 16-bit x 4-bank
- Programmable Mode registers
- CAS Latency: 2, or 3
- Burst Length: 1, 2, 4, 8, or full page
- Burst Type: interleaved or linear burst
- Burst stop function
- Auto Refresh and Self Refresh
- 4096 refresh cycles/64ms
- CKE power down mode
- Single +3.3V ± 0.3V power supply
- Interface: LVTTL
- 54-pin 400 mil plastic TSOP II package
- Pb free and Halogen free
- 60-ball 6.4mm x 10.1mm VFBGA package
- Pb free

7.3 Pin Configuration

Symbol	Type	Description
CLK	Input	**Clock:** CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CLK signal. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.
BA0,BA1	Input	**Bank Activate:** BA0, BA1 input select the bank for operation.

BA1	BA0	Select Bank
0	0	BANK #A
0	1	BANK #B
1	0	BANK #C
1	1	BANK #D

A0-A11	Input	**Address Inputs:** A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 2M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQM, UDQM	Input	**Data Input/Output Mask:** Controls output buffers in read mode and masks Input data in write mode.
DQ0-DQ15	Input / Output	**Data I/O:** The DQ0-15 input and output data are synchronized with the positive edges of CLK. The I/Os are maskable during Reads and Writes.
NC/RFU	-	**No Connect:** These pins should be left unconnected.
V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity. (3.3V± 0.3V)
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity. (0 V)
V_{DD}	Supply	**Power Supply:** +3.3V ± 0.3V
V_{SS}	Supply	**Ground**

8 S25FL016A - 16 Megabit Cmos 3.0 Volt Flash Memory with 50-Mhz (Serial Peripheral Interface)Bus

8.1 General Description

The S25FL016A is a 3.0 Volt (2.7V to 3.6V), single-power supply Flash memory device.The device consist of thirty-two sectors, each with 512 Kb memory.

The device accepts data written to SI (Serial Input) and outputs data on SO (Serial Output). The devices are designed to be programmed in-system with the standart 3.0 volt Vcc supply.

The memory can be programmed 1 to 256 bytes at a time, using the Page Praogram command. The device supports Sector Erase and Bulk Erase commands.

Each device requires only a 3.0 volt power supply (2.7V to 3.6V) for both read and write functions. Internally generated and regulated voltages are provided for the program oprerations. This device does not require a Vpp supply.

8.2 Distinctive Characteristics

Architectural Advantages

- **Single Power supply operation**

- Full voltage range: 2,7 to 3,6V read and program operations

- **Memory Architecture**

- Thirty-two sectors with 512 Kb each

- **Program**

- Page program (up to 256 bytes) in 1,4 ms (typical)
- Program operations are on a page by page basis

- **Erase**

- 0,5s typical sector erase time
- 10s typical bulk erase time

- **Cycling Endurance**

- 100,000 cycles per sector typical

- **Data Retantion**

- 20 Years Typical

- **Device ID**

- JEDEC standart two-byte electronic signature
- RES command one-byte electronic signature for backward compatibility

- **Process Technology**

- Manufactured on 0,20 µm MirrorBit process technology

- **Package Option**

- Industry standart pinout
- 16-pin SO package (300 mils)
- 8-pin SO package (208 mils)
- 8-Contact WSON Package (6x8 mm), Pb Free

Performance Characteristics

- Speed
- 50Mhz clock rate (miximum)
- Power Saving Standby Mode
- Standby Mode 50 µA (max)
- Deep Power Down Mode 1,3µA (typical)

Memory Protection Features

- **Memory Protection**

- W# pin works in conjuction with Status Register Bits to protect specified memory areas
- Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only

Software Features

SPI Bus Compatible Serial Interface

9 4M x 16 bit Synchronous DRAM (ANALOG SIDE SDRAM)

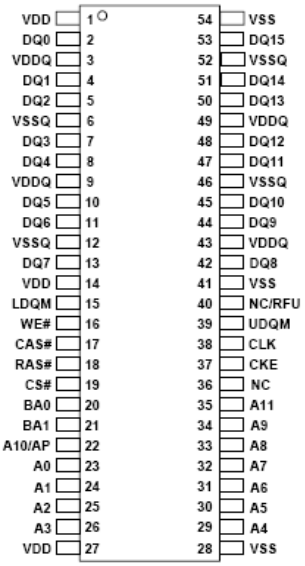
9.1 General Description

The EM638165 SDRAM is a high-speed CMOS synchronous DRAM containing 64Mbits. It is internally configured as 4 Banks of 1M word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a Bank Activate command which is then followed by a Read or Write command. The EM638165 provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications.

9.2 Features

• Fast access time from clock: 4.5/5/5.4 ns
• Fast clock rate: 200/166/143 MHz
• Fully synchronous operation
• Internal pipelined architecture
• 1M word x 16-bit x 4-bank
• Programmable Mode registers
- CAS Latency: 2, or 3
- Burst Length: 1, 2, 4, 8, or full page
- Burst Type: interleaved or linear burst
- Burst stop function
• Auto Refresh and Self Refresh
• 4096 refresh cycles/64ms
• CKE power down mode
• Single +3.3V ± 0.3V power supply
• Interface: LVTTL
• 54-pin 400 mil plastic TSOP II package
- Pb free and Halogen free
• 60-ball 6.4mm x 10.1mm VFBGA package
  - Pb free

9.3 Pinning



<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>CLK</td><td>Input</td><td>Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.</td></tr>
<tr><td>CKE</td><td>Input</td><td>Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.</td></tr>
<tr><td>BA0,BA1</td><td>Input</td><td>Bank Activate: BA0, BA1 input select the bank for operation.
<table>
<tr><th>BA1</th><th>BA0</th><th>Select Bank</th></tr>
<tr><td>0</td><td>0</td><td>BANK #A</td></tr>
<tr><td>0</td><td>1</td><td>BANK #B</td></tr>
<tr><td>1</td><td>0</td><td>BANK #C</td></tr>
<tr><td>1</td><td>1</td><td>BANK #D</td></tr>
</table></td></tr>
<tr><td>A0-A11</td><td>Input</td><td>Address Inputs: A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 1M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.</td></tr>
<tr><td>CS#</td><td>Input</td><td>Chip Select: CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.</td></tr>
<tr><td>RAS#</td><td>Input</td><td>Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.</td></tr>
<tr><td>CAS#</td><td>Input</td><td>Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."</td></tr>
<tr><td>WE#</td><td>Input</td><td>Write Enable: The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.</td></tr>
</table>

LDQM, UDQM	Input	**Data Input/Output Mask:** Controls output buffers in read mode and masks Input data in write mode.
DQ0-DQ15	Input / Output	**Data I/O:** The DQ0-15 input and output data are synchronized with the positive edges of CLK. The I/Os are maskable during Reads and Writes.
NC/RFU	-	**No Connect:** These pins should be left unconnected.
V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity. (3.3V± 0.3V)
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity. (0 V)
V_{DD}	Supply	**Power Supply:** +3.3V ± 0.3V
V_{SS}	Supply	**Ground**

10 POWER STAGE

MB45 has two power options which is changed according to TV size and number of lambs.

10.1 IPS 15 Option

IPS16 power board is used with 19" MB45TV set (2 lamp panel) and IPS17 power board is used with 22" MB45TV set (4 lamp panel). These are supplied 12V, 5V_stby and 5V panel supplies.
Also regulators, step-downs and mosfet generate 3V3, 3V3_Stby, 5V_Tuner and 1,25V_Stby voltages for other different part of the chassis.
Audio supply is 5V in this case.

Components	Max estimated consumption (mA)							
	1V25_STB	1V8_VCC	3V3_STB	5V_STB	3V3_VCC	5V_VCC	12V_VCC	Comment
TUNER						200		
MSTAR (Concept IC)	720 / 31		440 / 10		85			On/Stdby
24C02 (HDMI E2PROM)						5		
Preamplifier TL062+LM358							50	
PT2333 (Audio Amplifier)						1800		
CY8C21x34 I (Capacitive Function Button)				50				Optional
15"/19"/22"/23" Panels						1500	1000	Max
LED				16				
IR Receiver				5				
25F80 (1MB 85MHz Serial Flash)			25					
K4S161622E (8MB SD)					155			
24C64					3			
USB Connector Supply						500		
PI5V330						1		
CI Slot Supply						500		
CT216T		373			260	373		
W25X16 (2MB/4MB Flash)					25			
EM63X165 (8MB/16MB/32MB SD)					210			
DVD							500	

11 IC SPECIFICATIONS

11.1 8K Smart Serial EEPROM – 24C64

General Description

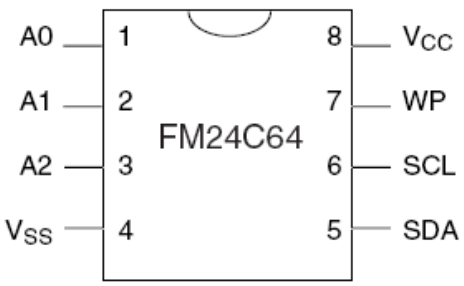
24C64 is a 64Kbit CMOS non-volatile serial EEPROM organized as 8K x 8 bit memory. This device confirms to Extended IIC 2-wire protocol that allows accessing of memory in excess of 16Kbit on an IIC bus. This serial communication protocol uses a Clock signal (SCL) and a Data signal (SDA) to synchronously clock data between a master (e.g. a microcontroller) and a slave (EEPROM). 24C64 is designed to minimize pin count and
simplify PC board layout requirements.

24C64 offers hardware write protection where by the entire memory array can be write protected by connecting WP pin to VCC. This section of memory then becomes unalterable until the WP pin is switched to VSS.

Features

 Extended operating voltage: 2.5V to 5.5V
 Up to 400 KHz clock frequency at 2.5V to 5.5V
 Low power consumption
—0.5mA active current typical
—10µA standby current typical
—1µA standby current typical (L version)
—0.1µA standby current typical (LZ version)
 Schmitt trigger inputs
 32 byte page write mode
 Self timed write cycle (6ms typical)
 Hardware Write Protection for the entire array
 Endurance: up to 100K data changes
 Data Retention: Greater than 40 years
 Packages: 8-Pin DIP, 8-Pin SO and 8-Pin TSSOP
 Temperature range
—Commercial: 0°C to +70°C
—Industrial (E): -40°C to +85°C
—Automotive (V): -40°C to +125°C

Pin Configuration



Pin Names

V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply
A0, A1, A2	Device Address Inputs

11.2 TL062

It is used as a pre-amplifer for scart audio output on MB45 main board.

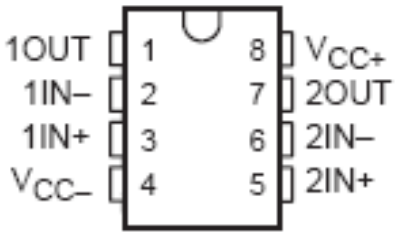
General Description

Low-power JFET-input operational amplifier

Features

- Very Low Power Consumption
- Typical Supply Current . . . 200 µA (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes VCC+
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/µs Typ

Pin Configuration



11.3 FSA3157

It is used for switching DVD_Y/C video signal and DVB_Y/C video signal on the MB45 mainboard, also there are two jumpers option for by-passing this switch.

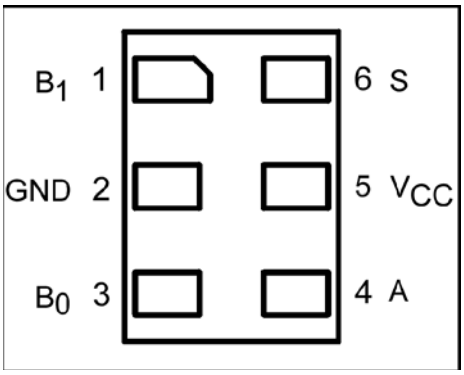
General Description

FSA3157 is a high performance, single-pole/double-throw (SPDT) Analog Switch or 2:1 Multiplexer/Demultiplexer Bus Switch. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance. The break before make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V VCC operating range. The control input tolerates voltages up to 5.5V independent of the VCC operating range.

Features

_ Useful in both analog and digital applications
_ Space saving SC70 6-lead surface mount package
_ Ultra small MicroPak leadless package
_ Low On Resistance; < 10Ω on typ @ 3.3V VCC
_ Broad VCC operating range; 1.65V to 5.5V
_ Rail-to-Rail signal handling
_ Power down high impedance control input
_ Overvoltage tolerance of control input to 7.0V
_ Break before make enable circuitry
_ 250 MHz - 3dB bandwidth

Pin Configuration



Pin Names	Description
A, B_0, B_1	Data Ports
S	Control Input

11.4 FDS8878

It is used for providing 5V tuner supply.

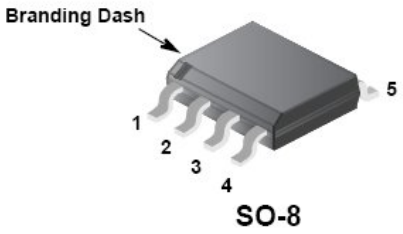
General Description

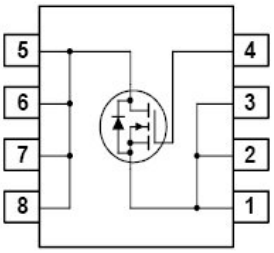
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low rDS(on) and fast switching speed.

Features

- rDS(on) = 14mΩ, VGS = 10V, ID = 10.2A
- rDS(on) = 17mΩ, VGS = 4.5V, ID = 9.3A
- High performance trench technology for extremely low rDS(on)
- Low gate charge
- High power and current handling capability
- RoHS Compliant

Pin Configuration





11.5 ST24LC21 (Optional)

ST24LC21 is an EEPROM which is used for storing the VGA output resolution information.

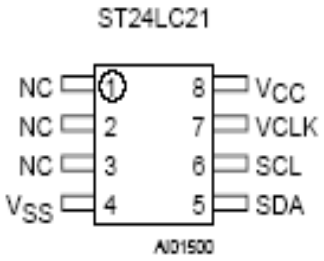
General Description

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 Bits.This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Features

- 1 Mıllıon Erase/Wrıte Cycles
- 40 Years Data Retentıon
- 2.5v To 5.5v Sıngle Supply Voltage
- 400k Hz Compatıbılıty Over The Full
- Range Of Supply Voltage
- Two Wıre Serıal Interface I2c Bus
- Compatıble
- Page Wrıte (Up To 8 Bytes)
- Byte, Random And Sequentıal Read
- Modes
- Self Tımed Programmıng Cycle
- Automatıc Address Incrementıng
- Enhanced Esd/Latch Up
- Performances

Pin Configuration



SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode
WC	Write Control

11.6 TDA1308T

TDA1308T is a class AB stereo headphone driver which is used as a headphone amplifier on MB45 mainboard.

General Description

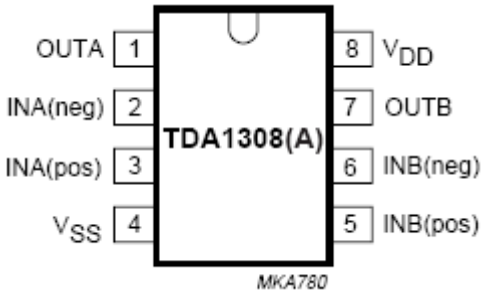
The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8, DIP8 or a TSSOP8 plastic package. The device is fabricated in a 1 mmCMOS process and has been primarily developed for portable digital audio applications.

Features

· Wide temperature range
· No switch ON/OFF clicks
· Excellent power supply ripple rejection

· Low power consumption
· Short-circuit resistant
· High performance
– high signal-to-noise ratio
– high slew rate
– low distortion
· Large output voltage swing.

Pin Configuration



SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
CD)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
V_{DD}	8	positive supply

11.7 STMP2161

STMP2161 is a current limiter which is used for switching the USB interface on MB45 mainboard.

General Description

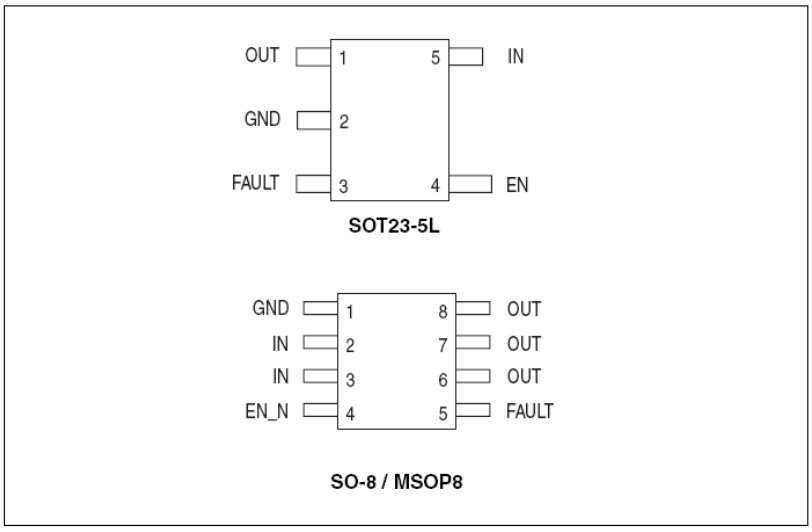
The STMPS2161 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporate 90 mΩ N-channel MOSFET high-side power switches for power-distribution. These switches are controlled by a logic enable input.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts the switch off to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until a valid input voltage is present.

Features

■ 90 mΩ high-side MOSFET switch
■ 500/1000 mA continuous current
■ Thermal and short-circuit protection with overcurrent logic output
■ Operating range from 2.7 V to 5.5 V
■ CMOS- and TTL-compatible enable inputs
■ Undervoltage lockout (UVLO)
■ 12 µA maximum standby supply current
■ Ambient temperature range, -40°C to 85°C
■ 8 kV ESD protection
■ Reverse current protection
■ Fault-blanking

Pin Configuration



Pin number			Name	Function
SO8	MSOP8	SOT23-5L		
1	1	2	GND	Ground
2	2	5	IN	2.7 V - 5.5 V input
3	3	-	IN	2.7 V - 5.5 V input
4	4	4	EN	Enable for power switch
5	5	3	FAULT	Open drain FAULT indicator, active low
6	6	1	OUT	Output of power switch
7	7	-	OUT	Output of power switch
8	8	-	OUT	Output of power switch

11.8 AZ1045

It is used for protecting the USB interface on MB45 mainboard.

General Description

AZ1045-04SU is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1045-04SU has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

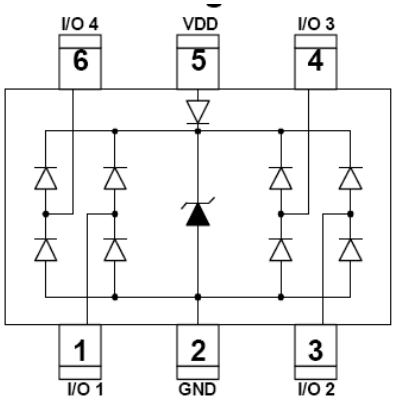
AZ1045-04SU is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components. Besides, there is a back-drive protection design in AZ1045-04SU for power-down mode operation. AZ1045-04SU may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Features

- ESD Protect for Transition Minimized Differential Signaling (TMDS) channels
- Protects four I/O lines and one VDD line
- Provide ESD protection for each channel to
  Revision 2008/01/23 ©2008 Amazing Micro. 1 www.amazingIC.com
  IEC 61000-4-2,(ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-5 (Lightning) 4.7A (8/20μs)
- For below 5V operating voltage
- Ultra low capacitance : 0.55pF typical
- 0.03pF matching capacitance between the TMDS intra-pair
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS diode

 Solid-state silicon-avalanche and active circuit triggering technology
 Back-drive protection for power-down mode
 Lead-free version available

Pin Configuration



ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs) (I/O pins)	I_{PP}	4.7	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Air) (I/O pins) ESD per IEC 61000-4-2 (Contact) (I/O pins)	V_{ESD_IO}	19 12	**kV**
ESD per IEC 61000-4-2 (Air) (VDD, GND pins) ESD per IEC 61000-4-2 (Contact) (VDD, GND pins)	V_{ESD_PW}	30 30	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

11.9 MP1583

MP1583 is a step-down regulator which is used for providing 3.3V DC from 12V DC and 5V Vcc from 12V.

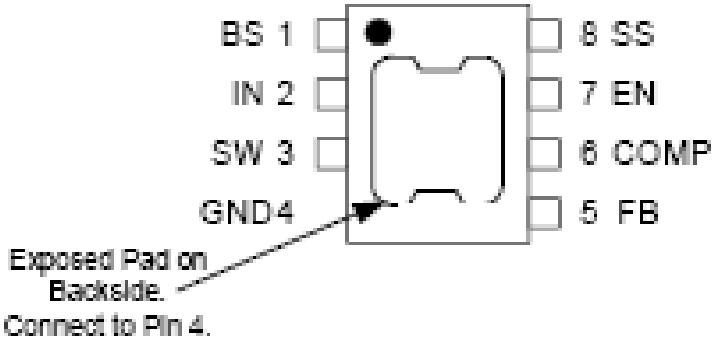
General Description

The MP1583 is a step-down regulator with a built in internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20μA of supply current.
The MP1583 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

Features

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20µA Shutdown Mode
- Fixed 385KHz frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 23V operating Input Range
- Output Adjustable From 1.22 to 21V
- Under Voltage Lockout
- Available in 8 pin SOIC Package
- 3A Evaluation Board Available

Pin Configuration



#	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side n-channel MOSFET switch. Connect a 4.7nF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. (Note: Connect the exposed pad on backside to Pin 4).
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.222V. See *Setting the Output Voltage*
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See *Compensation*
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. For automatic startup, leave EN unconnected.
8	SS	Soft Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.

11.10 LM1117

It is a regulator which is used for providing 1.8V from 3.3V for DVB side.

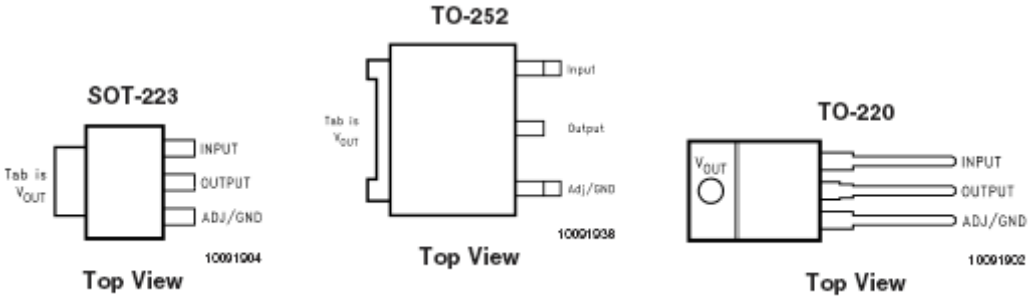
General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to as-sure output voltage accuracy to within ±1%. The LM1117 series is available in SOT- 223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

Pin Configuration



11.11 MP2109

It is a step-down converter which is used for seting the 1.26V STBY Output and 3.3V STBY Output.

General Description

The MP2109 contains two independent 1.2MHz constant frequency, current mode, PWM step-down converters. Each converter integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. The MP2109 is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) battery. Each converter can supply 800mA of load current from a 2.5V to 6V input voltage. The output voltage can be regulated as low as 0.6V. The MP2109 can also run at 100% duty cycle for low dropout applications.

Features

Up to 95% Efficiency

1.2MHz Constant Switching Frequency

800mA Load Current on Each Channel

2.5V to 6V Input Voltage Range

Output Voltage as Low as 0.6V

100% Duty Cycle in Dropout

Current Mode Control

Short Circuit Protection

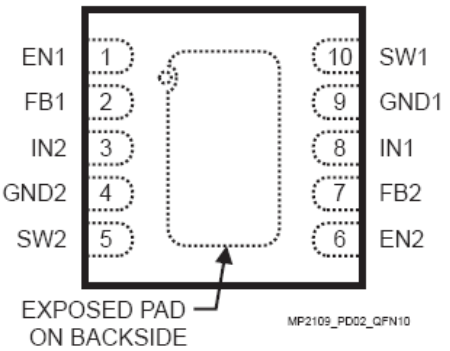
Thermal Fault Protection

<0.1μA Shutdown Current

Internally Compensated

Space Saving 10-Pin QFN Package

Pin Configuration



Pin #	Name	Description
1	EN1	Channel 1 Enable Control Input. Drive EN1 above 1.5V to turn on the Channel 1. Drive EN1 below 0.3V to turn it off (shutdown current < 0.1µA).
2	FB1	Channel 1 Feedback Input. Connect FB1 to the center point of the external resistor divider. The feedback voltage is 0.6V.
3	IN2	Channel 2 Supply Input. Bypass to GND with a 2.2µF or greater ceramic capacitor.
4	GND2	Ground 2.
5	SW2	Channel 2 Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.
6	EN2	Channel 2 Enable Control Input. Drive EN2 above 1.5V to turn on the Channel 2. Drive EN2 below 0.3V to turn it off (shutdown current < 0.1µA).
7	FB2	Channel 2 Feedback Input. Connect FB2 to the center point of the external resistor divider. The feedback voltage is 0.6V.
8	IN1	Channel 1 Supply Input. Bypass to GND with a 2.2µF or greater ceramic capacitor.
9	GND1	Ground 1.
10	SW1	Channel 1 Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.

11.12 FDC642P

FDC642P is a p-channel mosfet which is used for switching the panel supply.

General Description

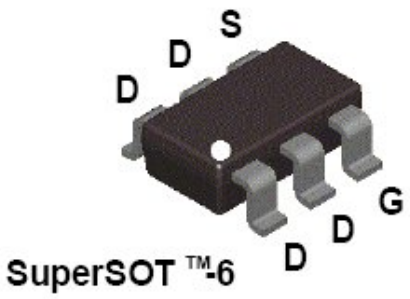
This P-channel 2.5V specified MOSFET is produced using advanced PowerTrench process that has been especially tailored to minimize on state resistance and yet maintain low gate charge for superior switching performance.

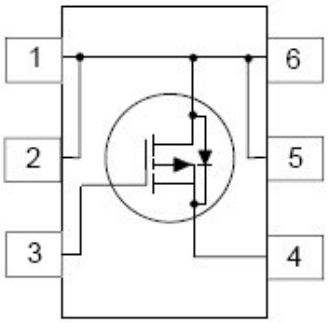
These devices have been design to offer exceptional power dissipation in a very small footprint for applications where larger packages are impractical.

Features

- Fast switching speed.
- -4 A,-20V. $R_{DS(on)}$ = 0.065 ohm @ V_{GS}=-4.5V
  $R_{DS(on)}$ = 0.100 ohm @ V_{GS}=-2.5V
- Low gate charge (7.2nC typical).
- High performance trench technology for extremely low $R_{DS(on)}$
- SuperSOT-6 package:small footprint (72% smaller than Standard SO-8;low profile (1mm thick).

Pin Configuration





11.13 XC5000 (Optional)

XC50000 is a RF to Baseband Silicon Tuner and the usage of XC5000 is optional on MB45TV set.

General Description

The Single-Chip Multi-Standard Tuner + VIF/SIF XC5000 supports all analog TV formats transmitted worldwide in the 42-864 MHz band on either cable or terrestrial broadcast channels. It implements on-chip tuning, channel filtering and demodulation, without external (SAW) filters and has no manually tunable parts. The broadband tuner converts the selected channel into an Intermediate Frequency (IF), which is then sampled by an internal high-resolution analog-to-digital converter (A/D) for further processing. For analog broadcast standards the video signal is demodulated and output as a composite video base-band signal (CVBS) through a high-performance smoothing filter. The sound carrier is filtered and output as a 2nd Sound IF (SIF) or demodulated and output as a mono TV sound. In DTV mode, the Digital TV signals are filtered using a standard-dependent high-rejection channel fitler and converted to a user-programmable output frequency. At the output of the D/A converter, the DTV signal is low-pass filtered using a high-performance smoothing filter and input to a variable gain amplifier. The amplifier gain can be controlled via an external analog signal on Vagc.

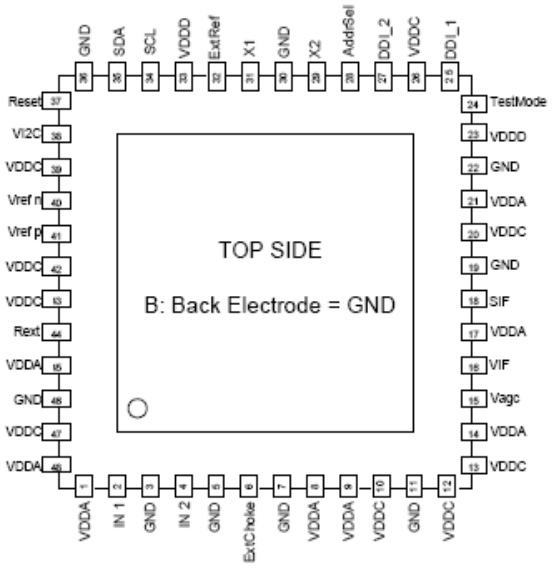
Features

_ Standard specific digital picture carrier recovery:
Alignment-free
Quartz-stable and accurate
No externally tunable parts
_ Multi-standard RF-to-baseband receiver
_ Integrated RF PLL filter reducing risk of noise pickup on the board
_ Standard specific digital video/audio splitting
_ Integrated DSP for high quality demodulation both in analog and digital modes
_ Integrated smoothing filters for CVBS output (analog mode) and IF-output (digital mode)
_ Supports DDI (digital direct interface) interfacing to the digital demodulator equipped with DDI, eliminating the quantization noise (from DAC/ADC).
_ Onboard digital processing for the following analog standards: B/G, D/K, I, L/L' and M/N
_ Inter-carrier sound output or mono analog sound direct output

_ Mono analog sound demodulation for both AM (SECAM L/L') and FM, including de emphasis
_ Compatible with a wide variety of signal conditions, including video overmodulation, airplane flutter and nonstandard sound.
_ DTV Mode for operation with external DTV demodulator. XC5000 applies filters and converts signal to arbitrary output frequency. Supports standards such as ATSC, OpenCable, DVB-C, DVB-T, ISDB-T, DMB-TH.
_ Excellent adjacent channel rejection
_ Low noise and excellent SNR
_ Dual input capability to address both TV and FM radio reception
_ Controlled via I2C-bus, up to four units on the I2C bus via address select pin
_ 42 to 864 MHz input frequency range
_ Low power dissipation
_ Small footprint, QFN48
_ Lead-free manufacturing

The Single-Chip Multi-Standard Tuner plus VIF/SIF, XC5000 combines both tuning and demodulation functions for worldwide cable and terrestrial analog TV in one small package. It also includes high performance filtering and frequency-conversion functions for DTV with an external demodulator through LOW-IF or DDI. The XC5000's integrated tuner is based on proprietary tunable wideband active RF filtering technology that eliminates the need for special external components. The XC5000's high sensitivity, coupled with at least 65 dB image rejection makes it ideal for antenna and cable reception. The XC5000's integrated digital demodulation for analog TV performs the entire multi-standard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, generation of the 2nd sound IF (SIF) or mono TV sound for all worldwide standards. The XC5000 provides two inputs to address both TV and FM radio reception. Xceive's breakthrough patent-pending technology provides a powerful combination of high dynamic range with a large tunable range uniquely enabling superior pictures from off-air and cable applications. Supported formats include NTSC, PAL and SECAM. The XC5000 also supports most DTV standards including ATSC/8-VSB, OpenCable DVB-C, QAM64 & QAM256, DVB-T, ISDB-T and DBM-TH, and is compatible with most digital demodulators on the market today.

Pin Configuration



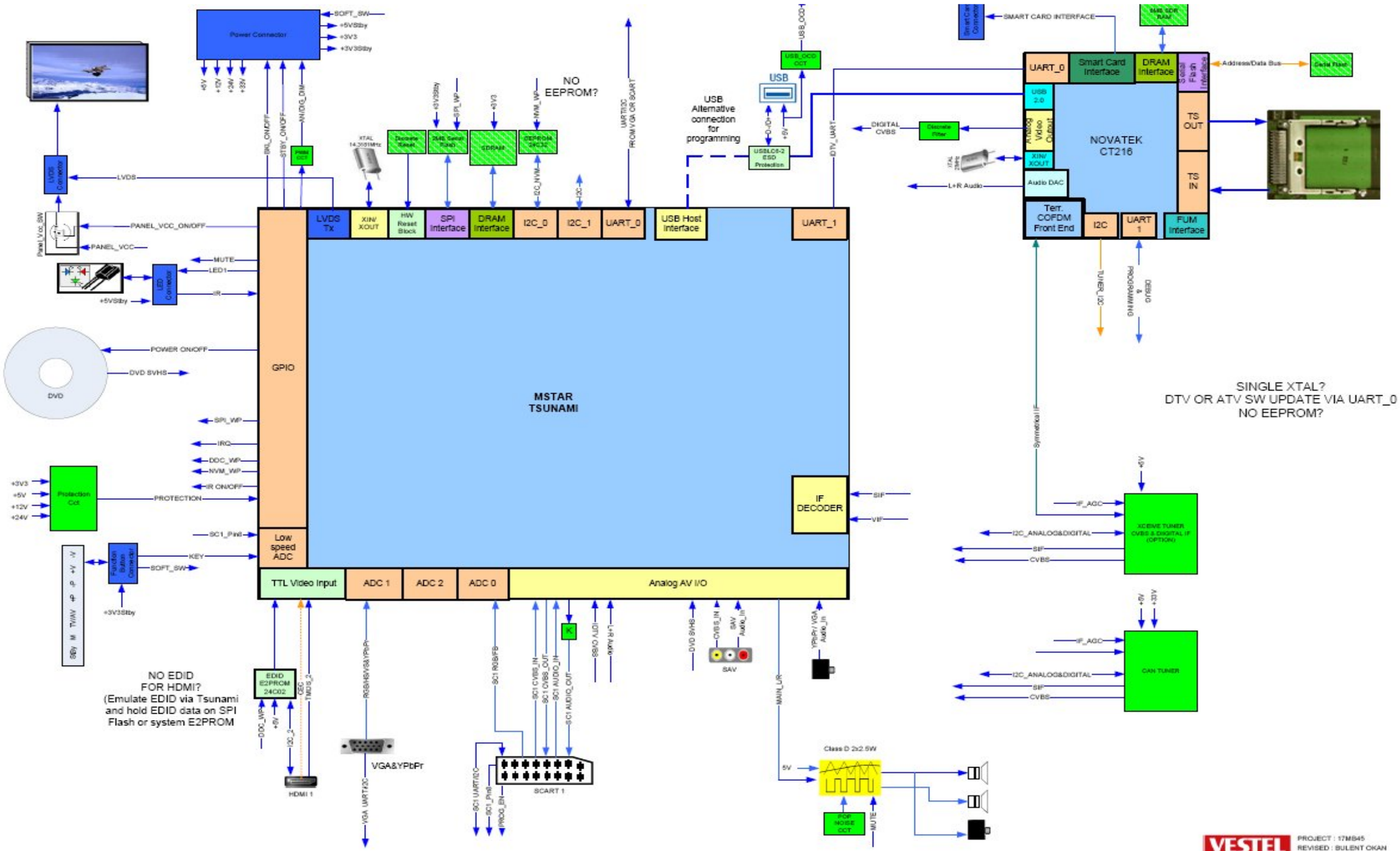
#	Name	Type	Description
B	GNDA	S	Main analog ground
1	VDDA	S	3.3V supply
2	IN1	RF/I	RF input 1; connected to GND through 390nH inductor.
3	GND	S	Ground
4	IN2	RF/I	RF input 2 (as secondary input for FM radio. Connect to ground if unused)
5	GND	S	Ground
6	ExtChoke	RF	External low-VHF choke inductor. 820nH against VDDA
7	GND	S	Ground
8	VDDA	S	3.3V supply
9	VDDA	S	3.3V supply

10	VDDC	S	1.8V supply (Mixed-signal)
11	GND	S	Ground
12	VDDC	S	1.8V supply (mixed-signal)
13	VDDC	S	1.8V supply (mixed-signal)
14	VDDA	S	3.3V supply (main analog)
15	Vagc	A/I	Control voltage of output AGC (digital reception)
16	VIF	A/O	Analog reception: CVBS Digital reception: Positive IF signal to digital demodulator
17	VDDA	S	3.3V supply
18	SIF	A/O	Analog reception: IF sound or baseband mono sound Digital reception: Negative IF signal to digital demodulator
19	GND	S	Ground
20	VDDC	S	1.8V supply (mixed-signal)
21	VDDA	S	3.3V supply
22	GND	S	Ground
23	VDDD	S	1.8V supply (DSP-digital)
24	TestMode	D/I	Used for production tests only. Do not connect.
25	DDI_1	D/O	DDI differential output, Negative
26	VDDC	D/S	1.8V supply (Mixed-signal)
27	DDI_2	D/O	DDI differential output, Positive
28	AddrSel	A/I	Select I^2C address; internal 1MΩ pull-down. Selection among 4 addresses if the pin is externally set at 0; VDDA/3;2VDDA/3;VDDA
29	X2	A	External crystal
30	GND	A	Ground
31	X1	A	External crystal
32	ExtRef	D/I	Ext. ref. frequency (1.8V or 3.3V; internal pull-down). Supersedes internal oscillator if a valid clock signal is provided. Do not connect for typical applications, if internal crystal oscillator is used.
33	VDDD	S	1.8V supply (DSP-digital)
34	SCL	D	I^2C SCL signal (clock; open drain; 5V compliant)
35	SDA	D	I^2C SDA signal (data; open drain; 5V compliant)
36	GND	S	Ground
37	Reset	D/I	Reset; active low; pull-up (3.3V). In test mode: select operation 1mS Reset duration is recommended after power-on
38	VI2C	S	3.3V or 5V I^2C voltage. Must be 5V for I^2C 5V compliance.
39	VDDC	S	1.8V supply (mixed-signal)
40	Vrefn	A	Negative reference voltage for ADC
41	Vrefp	A	Positive reference voltage for ADC
42	VDDC	S	1.8V supply (mixed-signal)
43	VDDC	S	1.8V supply (mixed-signal)
44	Rext	A	External reference resistor; connected to a 4.99kΩ resistor against GNDA
45	VDDA	S	3.3V supply (main analog)
46	GND	S	Ground
47	VDDC	S	1.8V supply (mixed-signal)
48	VDDA	S	3.3V supply

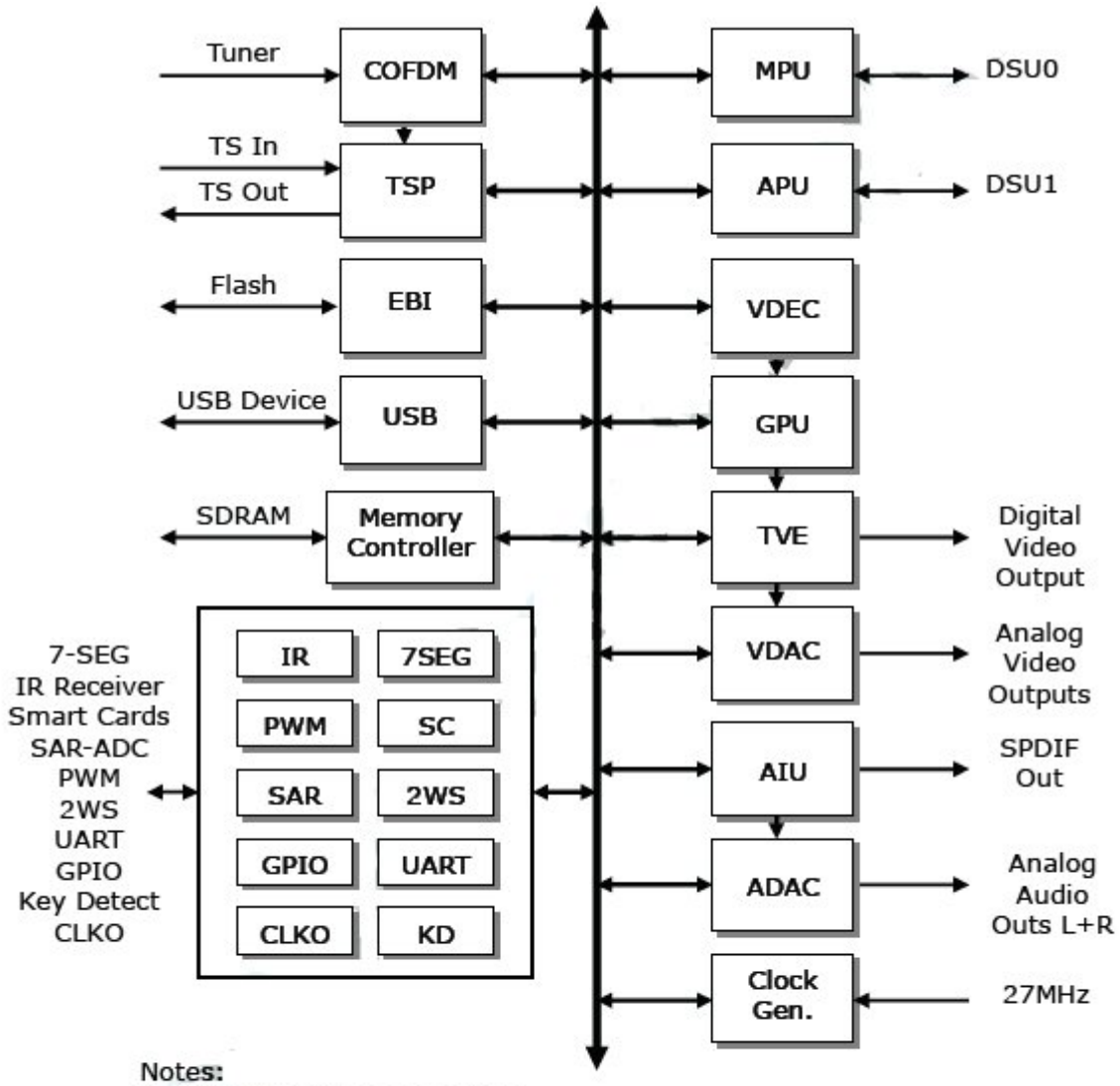
* When FM reception is not required, the Pin#4 should be connected to GND (Pin#3)

12 BLOCK DIAGRAMS

12.1 General Block Diagram

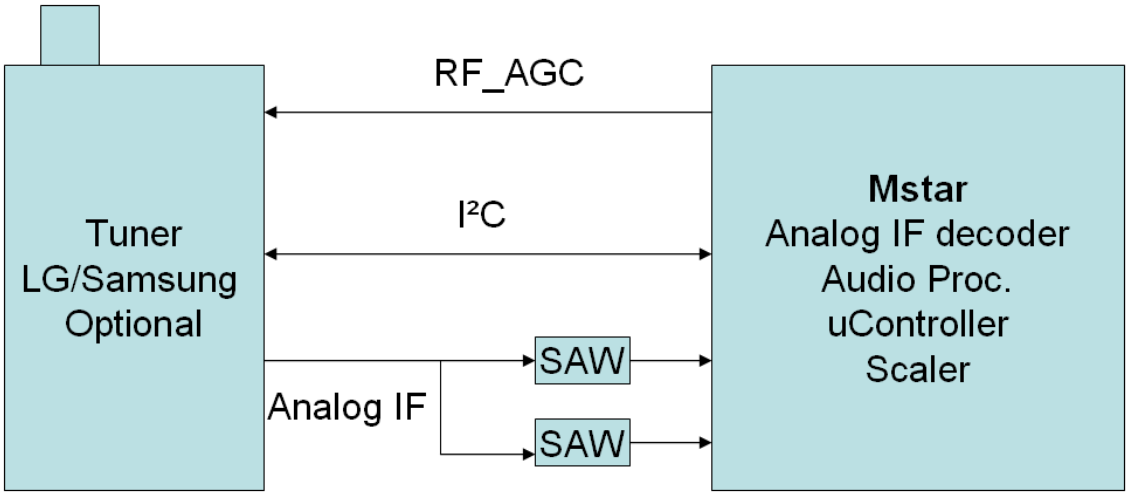


12.2 Integrated DVB-T Receiver Block Diagram

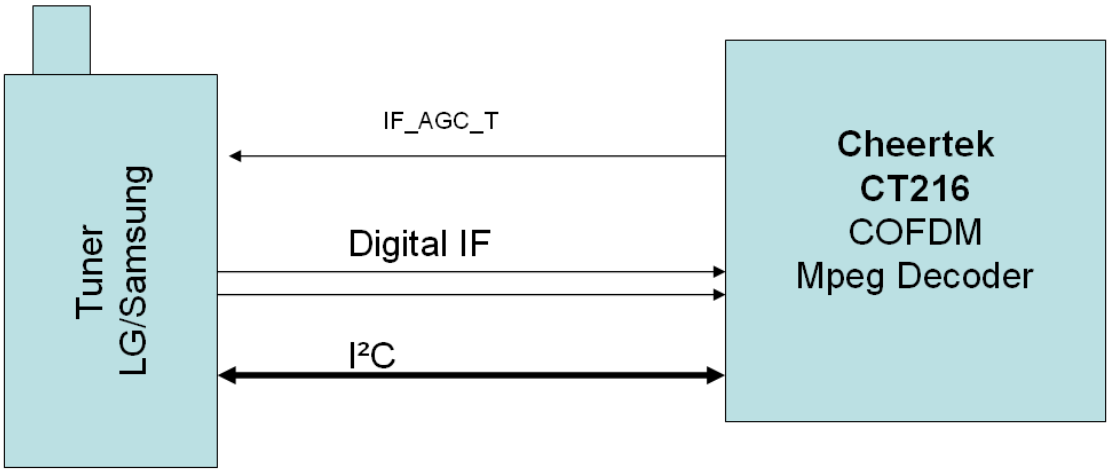


Notes:
1. APU: Audio Processor Unit
2. TSP: Transport Stream Processor
3. AIU: Audio Interface Unit
4. VDEC: Video Decoder
5. GPU: Graphics Processing Unit
6. EBI: Extended Bus Interface

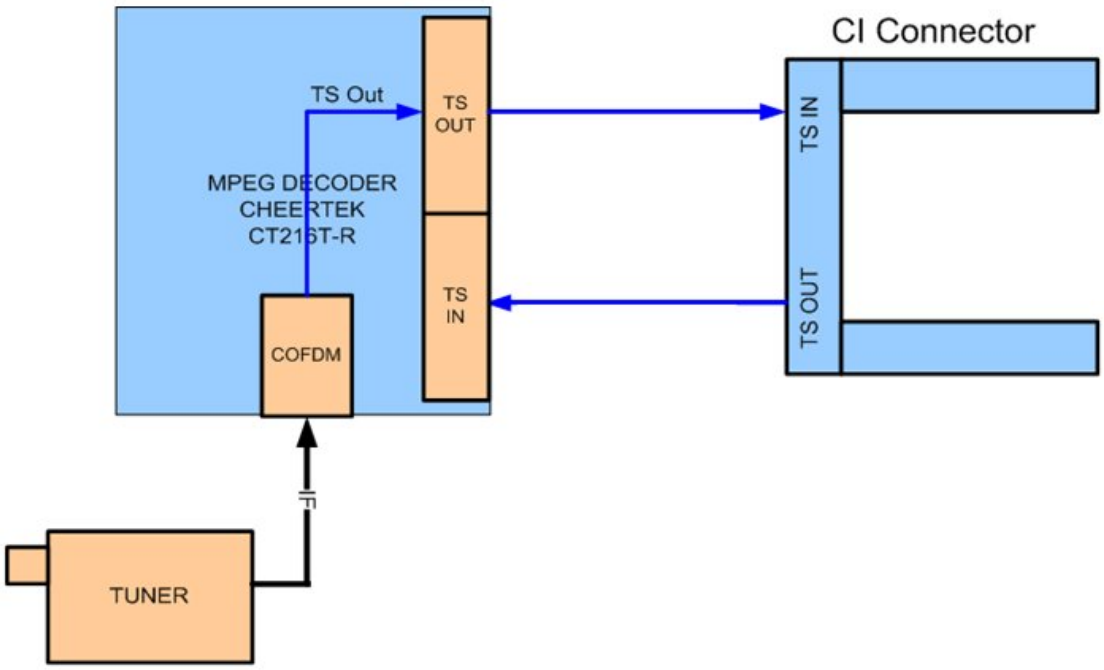
12.3 17MB45 Analog Front-End



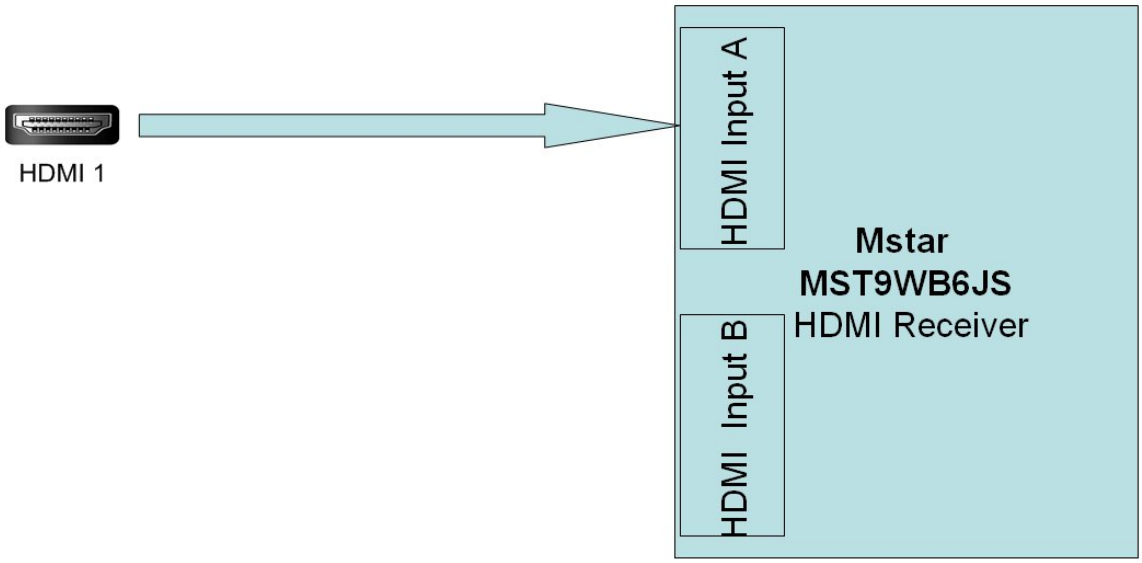
12.4 17MB45 Digital Front-End



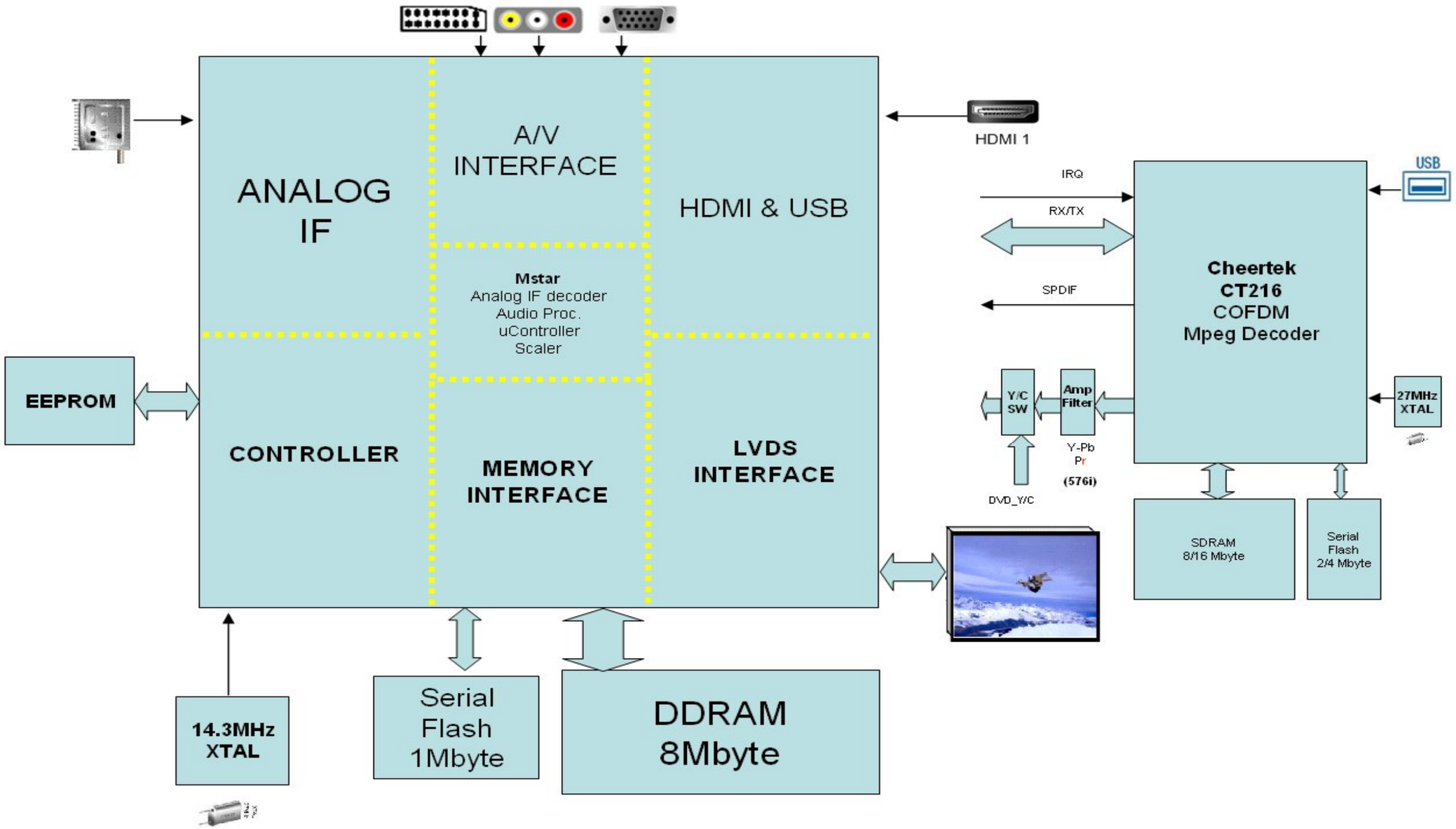
12.5 17MB45 Digital CI ve Smart Card Interface



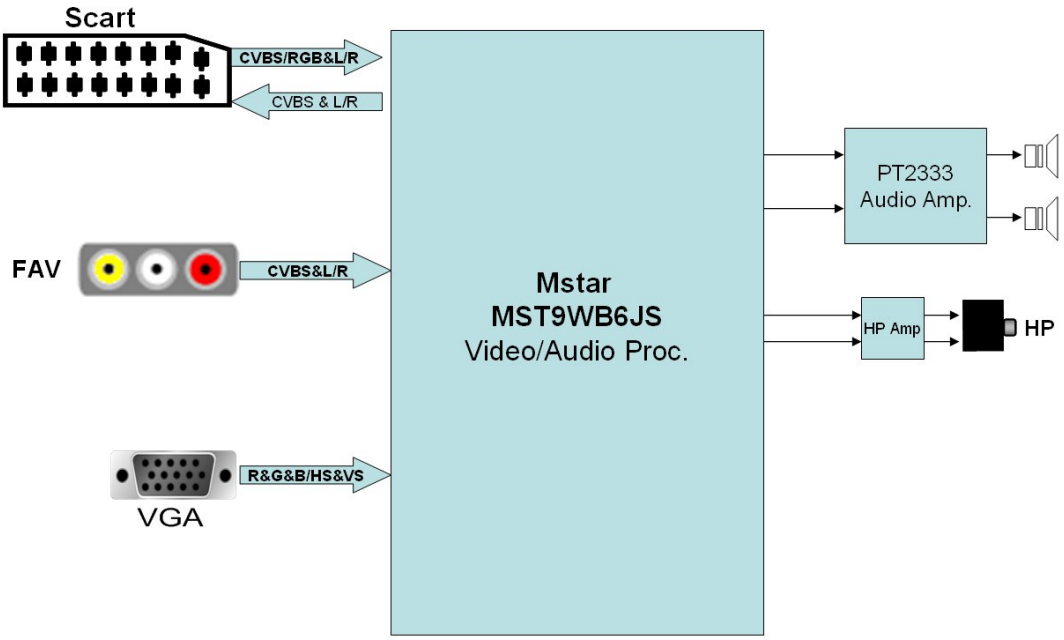
12.6 17MB45 HDMI Inputs



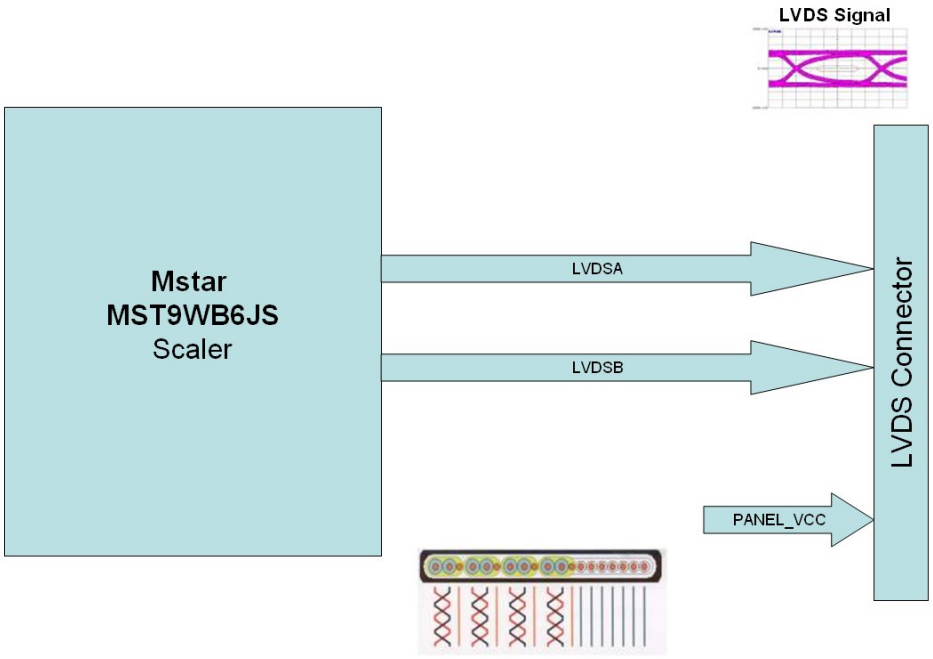
12.7 17MB45 Analog Interface " MSTAR IC "



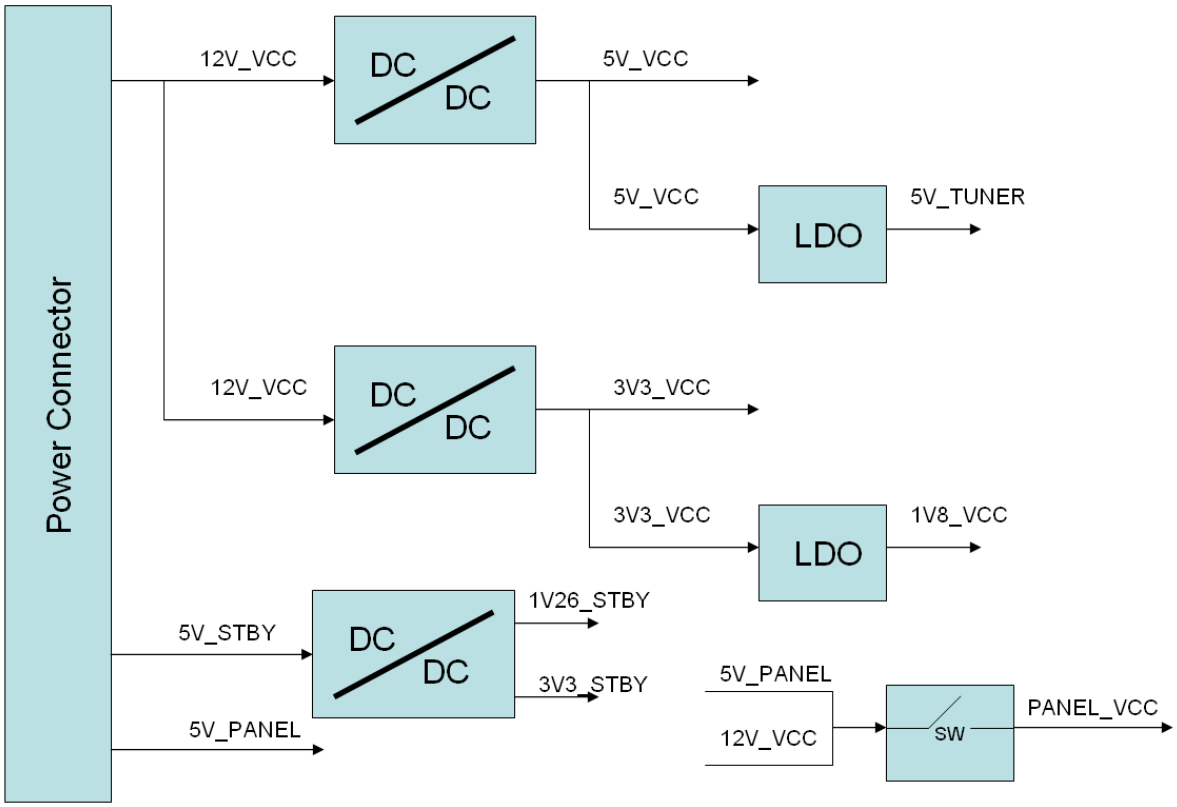
12.8 17MB45 Analog Input / Output



12.9 17MB45 LVDS Output



12.10 17MB45 Power



SOFTWARE UPDATE DESCRIPTION

1. MB45 Analog Part Software Update With Bootloader Procedure

1..1 The File Types Used By The Bootloader

All file types that used by the bootloader software are listed below:

1. The Binary File : It has ".bin" extension and it is the tv application. Its size is 1920 Kb.

2. The Config Binary File : It has ".cin extension and it is the config of the tv application. Its size may be 64 Kb or a few times 64 Kb.

3. The Test Script File : It has ".txt" extension and it is the test script that is parsed and executed by the bootloader. It don't have to be any times of 64 Kb.

4. The Test Binary File : It has ".tin" extension and it is used and written by the test groups. It is run to understand the problem part of the hardware.

Alltough a file that is used by the bootloader can be had any one of these extensions, its name has to be "VESTEL_S" and it has to be located in the root directory of the usb device.

1..2 Usage of The Bootloader

1) The starting to pass through : The chassis is only powered up.

2) The starting to download something : When chassis is powered up the menu key has to be pushed.Before the chassis is powered up and if any usb device is plugged to the usb port, the programme is downloaded from usb firstly. Any usb device is plugged to usb port , user must open hyperterminal in the pc and connect pc to chassis via Mstar debug tool and any one of scart,dsub9 or I2c connectors.

Serial connection settings are listed below:

- Bit per second: 115200
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

In this case the bootloader sofware puts "C" character to uart. After repeating "C" characters are seen in the hyperterminal user can send any file to chassis by selecting

Transfer -> Send File menu item and choosing "1K Xmodem" from protocol section.

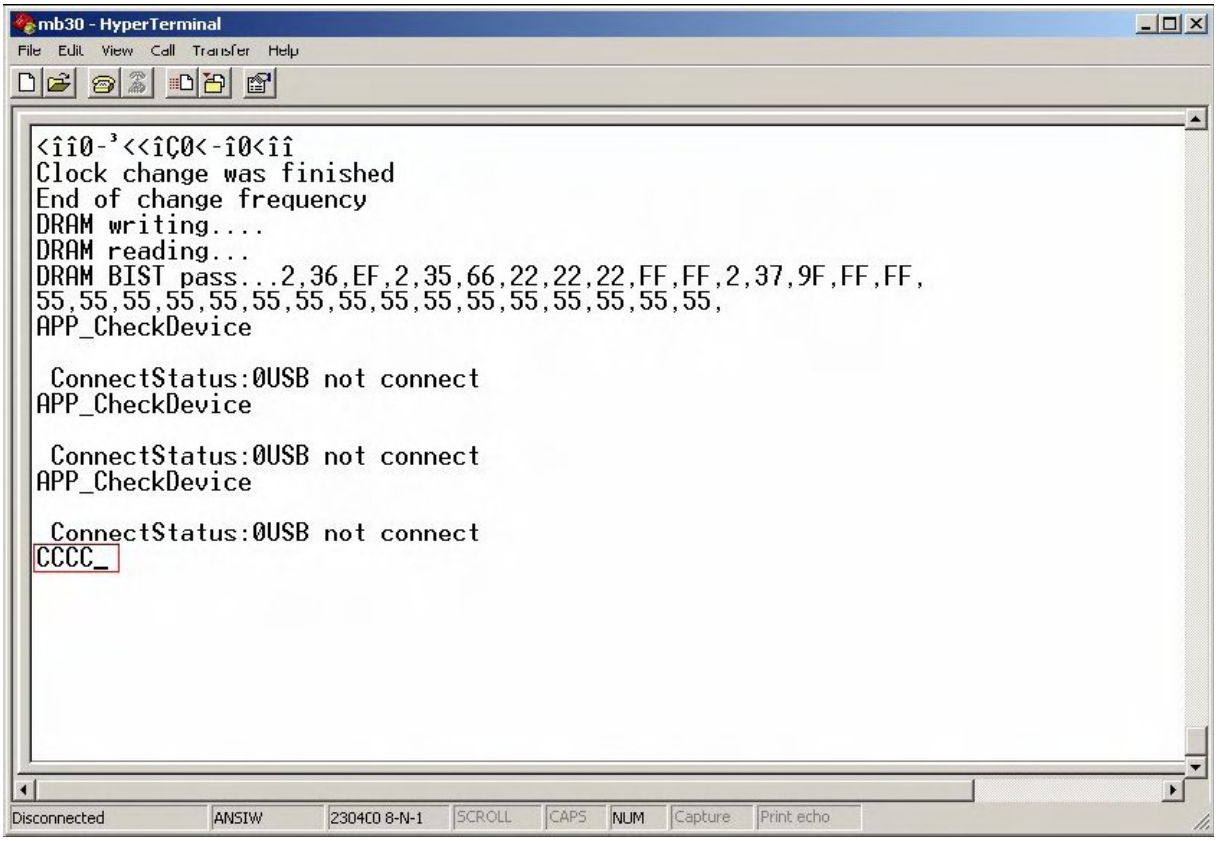


Figure 1. The Sample Output Before Sending The File

1..3 EEProm Update

To Update eeprom content via uart scart,dsub9 or i2c with Mstar tool can used.
Serial connection settings are listed below:

- Bit per second: 9600
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Programming menu item is choosed in the service menu and switch “HDCP Key Update Mode” from off to on.

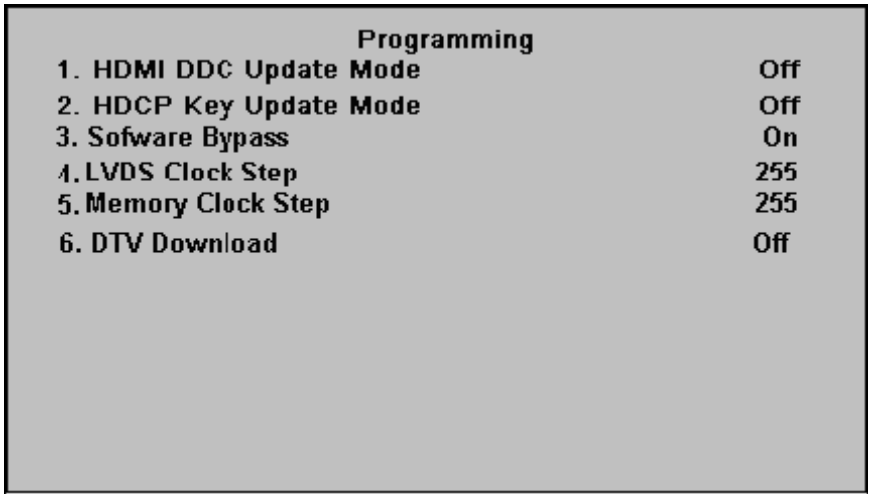


Figure 2. The Programming Service Menu

After then you must see Xmodem menu in the hyperterminal.To download hdcp key press k or to download eeprom content press w.

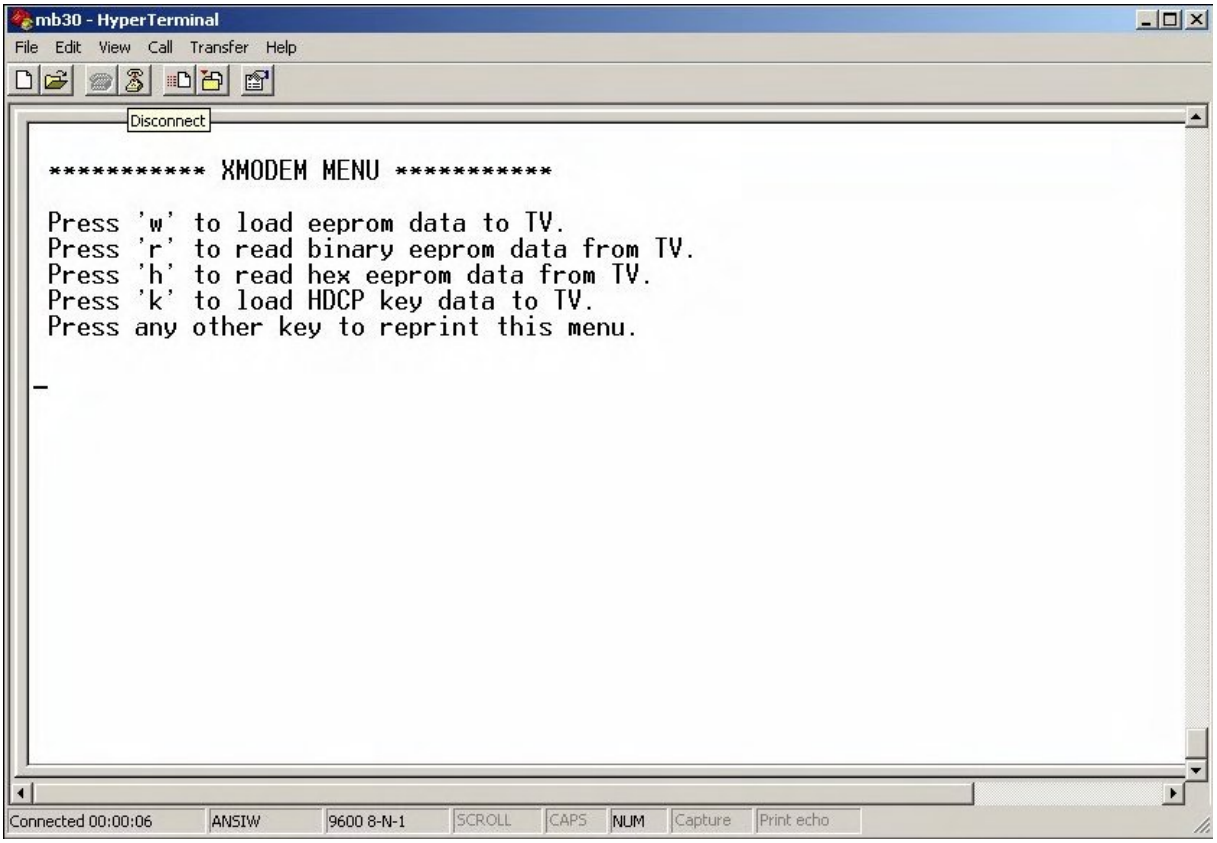


Figure 3. Xmodem Menu

If the repeated “C” characters are seen you can transfer file content via select Transfer->Send File and choose “**Xmodem”** protocol and click the “Send” button.

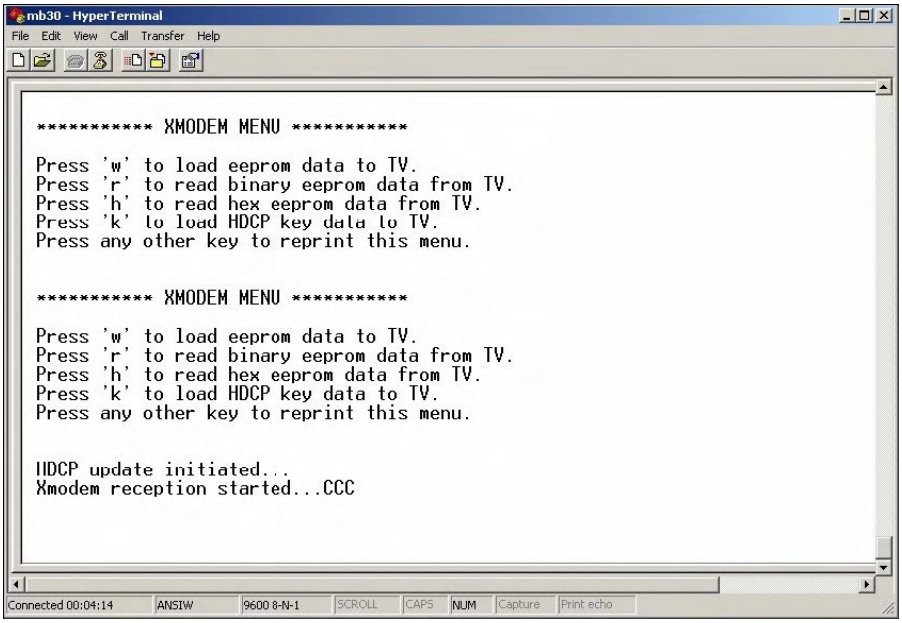


Figure 4. The Starting To Send

1..4 HDCP Key Upload Procedure

1) Turn on TV set.
2) Open a COM connection using fallowing parameters and select ISP COM Port No

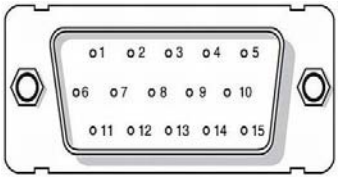
- Baud Rate: 9600 bps
- Data Bits: 8
- Stop Bits: 1
- Parity: None
- Flow Control: None

3) Enter service menu by pressing “4” “7” “2” 5” consecutively while main menu is open
4) Select “9. Programming”
5) Select “HDMI HDCP Update Mode” yes.
6) On Hyper Terminal Window press “k”
7) Click on send file under Transfer Tab.
8) Select Xmodem and choose the HDCP key to be uploaded.
9) Press send button
10)Restart TV set

2. MB45 Digital Part Software Update

2..1 MB45 Digital Software Update From VGA

Usage of VGA Pins:



Pin 4: RXD0
Pin 11: TXD0
Pin 8: Ground

Adjusting DTV Download Mode:

1. Power on the TV.
2. Exit the Stby Mode.

Adjusting HyperTerminal:

1. Connect the “MB45 VGA Interface” to VGA.
2. Also connect the “MB45 VGA Interface” to PC.
3. Open “HyperTerminal”.
4. Determine the “COM” settings listed and showed below.
    - Bit per second: 115200
    - Data bits: 8
    - Parity: None
    - Stop bits: 1
    - Flow control: None

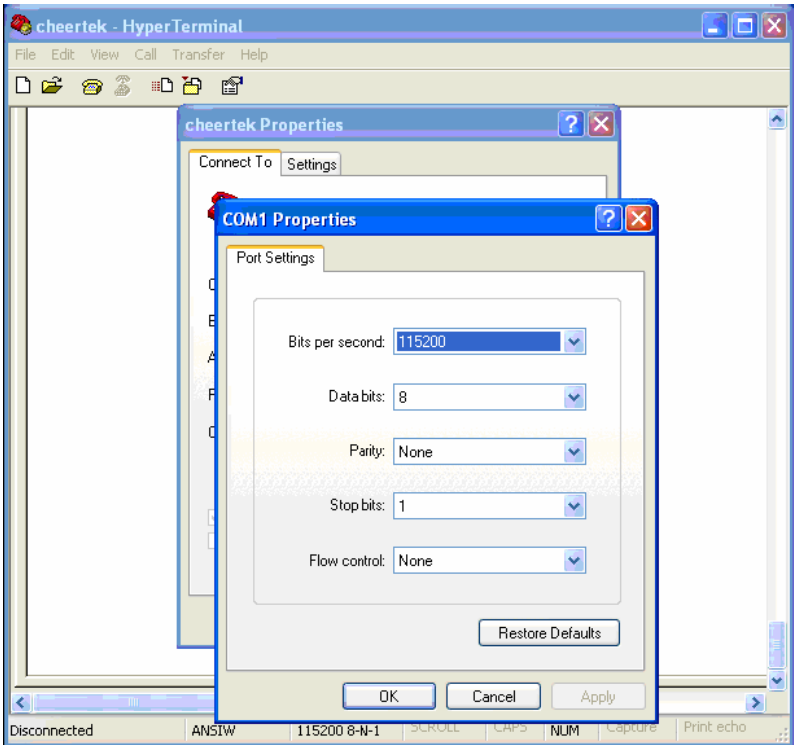


Figure 5.COM Properties Window

5. Click “OK”.

Software Updating Procedure

1. In the HyperTerminal Menu, click the “Connect” button.
2. Exit the Stby Mode.
3. The “Space” button on the keyboard must be pressed, when the following window can be seen.

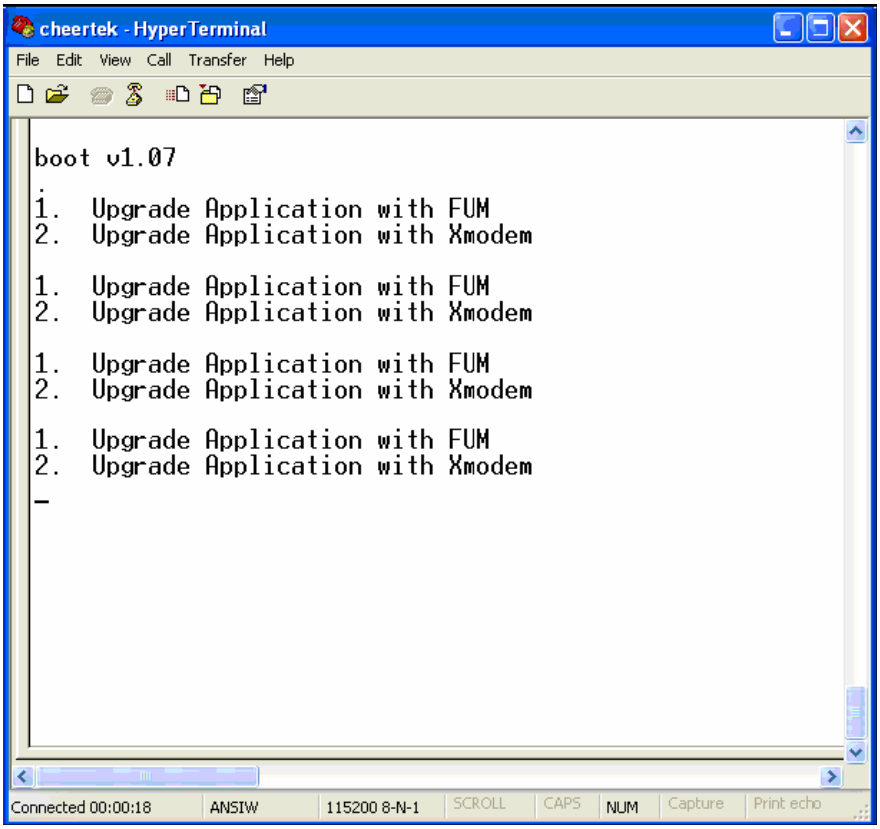


Figure 6.Selection Window

4. Press the “2” button on the keyboard for choosing “2. Upgrade Application with Xmodem”.
5. Repeating “C” characters are seen in the “HyperTerminal” menu.

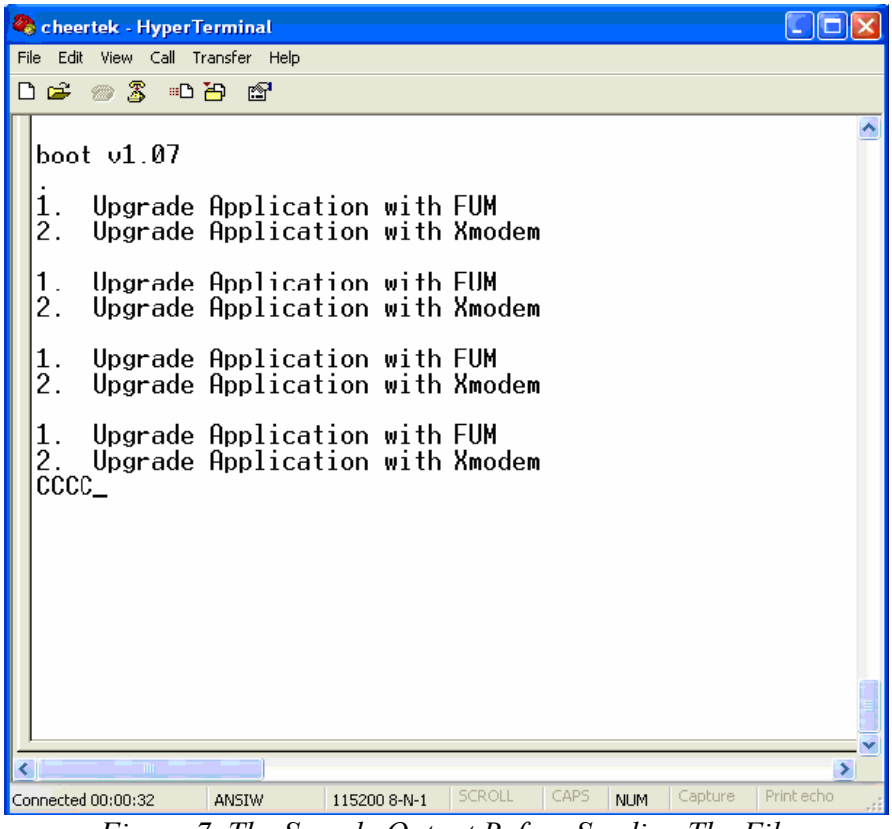


Figure 7. The Sample Output Before Sending The File

6. Click the “Send” button on the HyperTerminal
7. Select the “Filename **xxxx**_slot1.img” using “Browse”.
8. Choose the “1K Xmodem” from “Protocol” option.

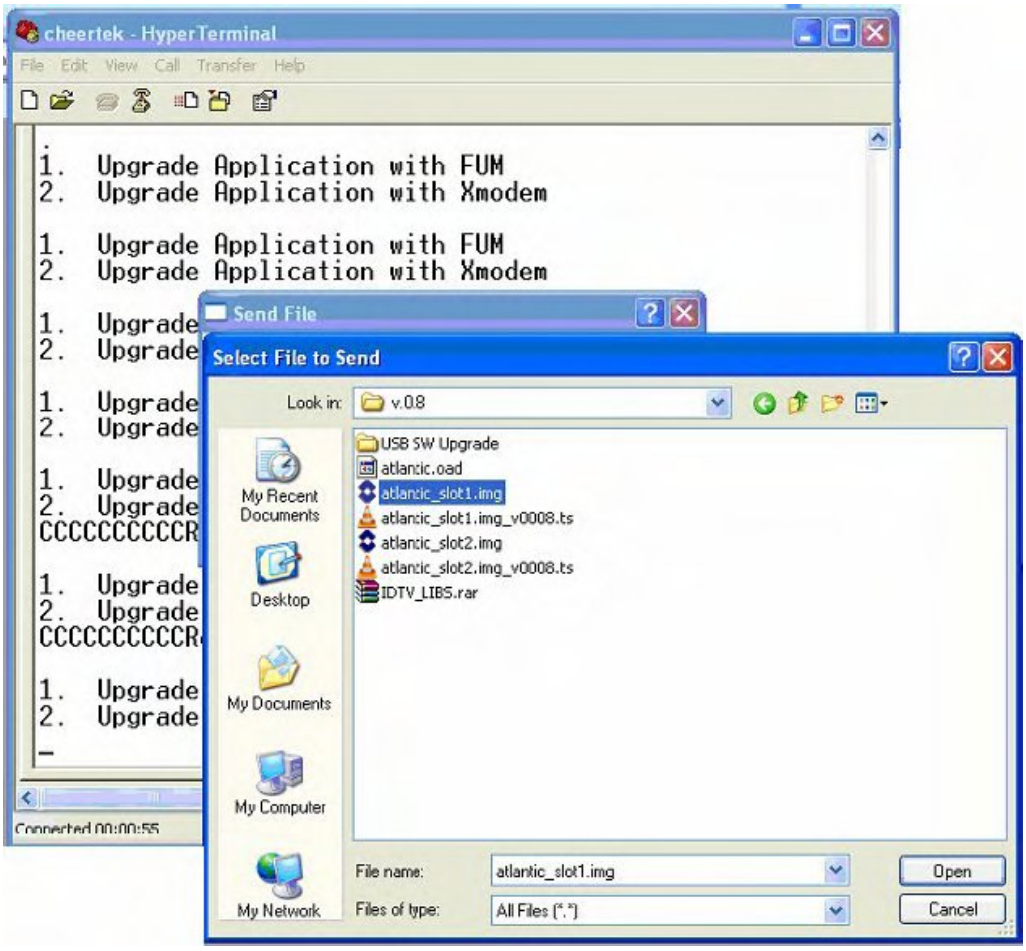


Figure 8. Selection of File

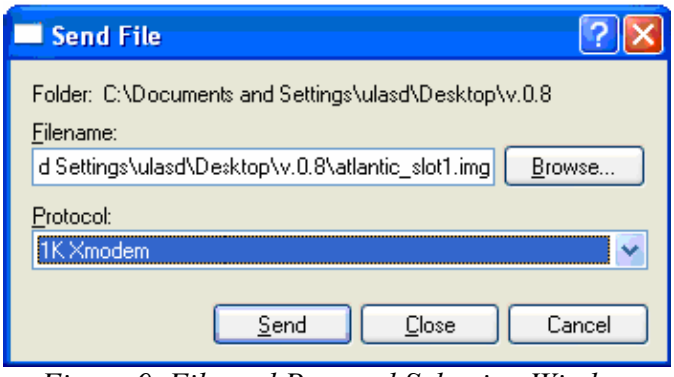


Figure 9. File and Protocol Selection Window

Note: In the Software updating Procedure section, when the first “C” character is seen, the filename selection process must be finished before 10 seconds. If the process can not be finished, the file sending operation will be cancelled. The following figure shows this situation.

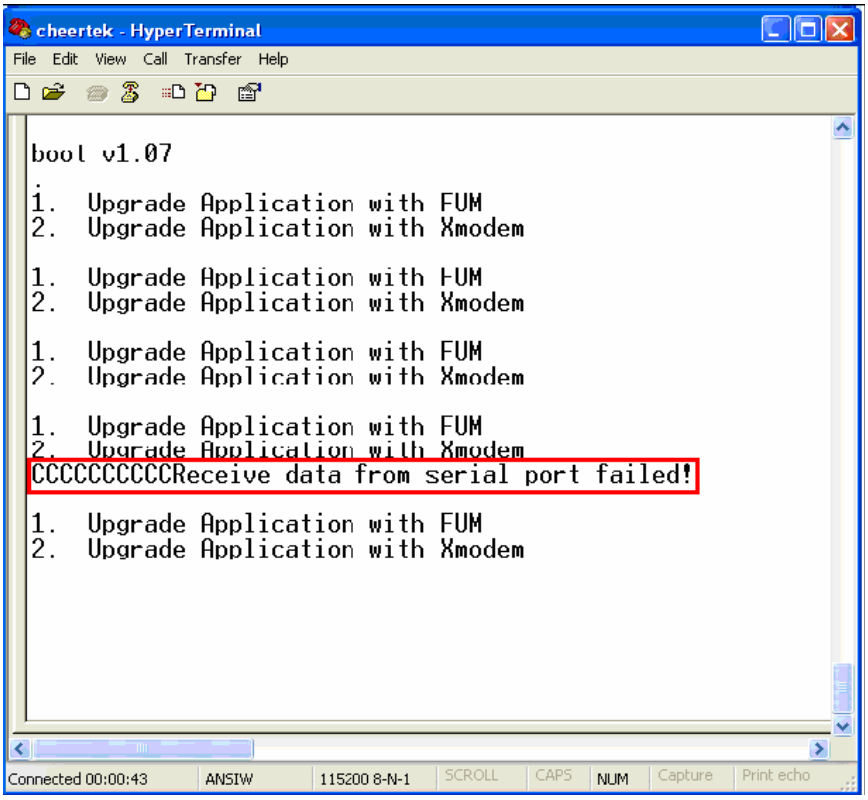


Figure 10. Capture of Receving Data Failing

9. When sending the file the following window must be seen.

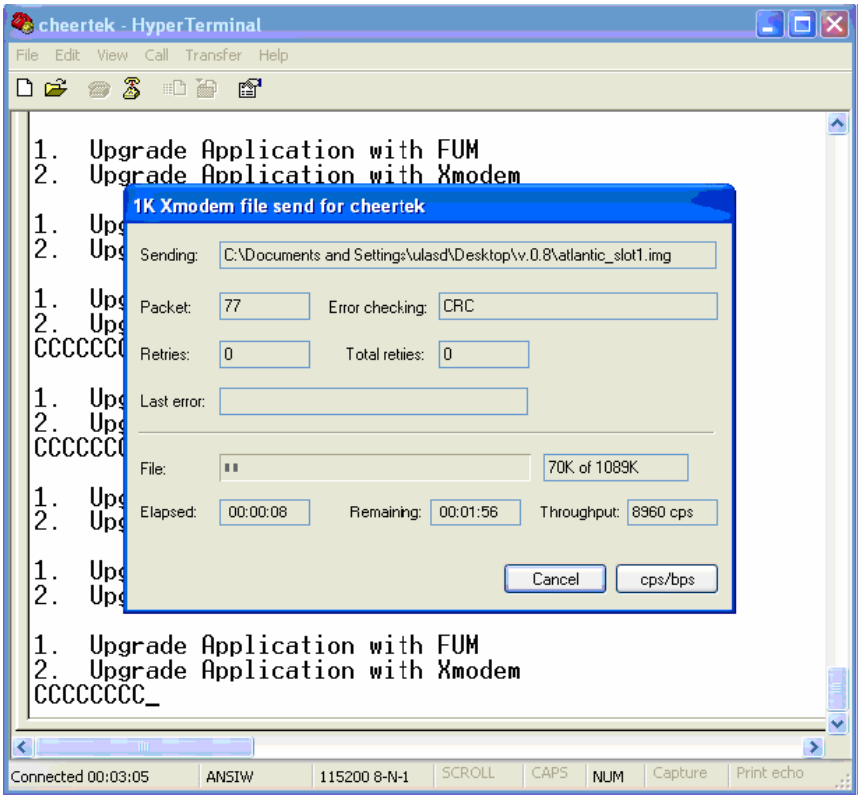


Figure 11. Capture of Sending Process

10. After the sending process the following HyperTerminal window must be seen.

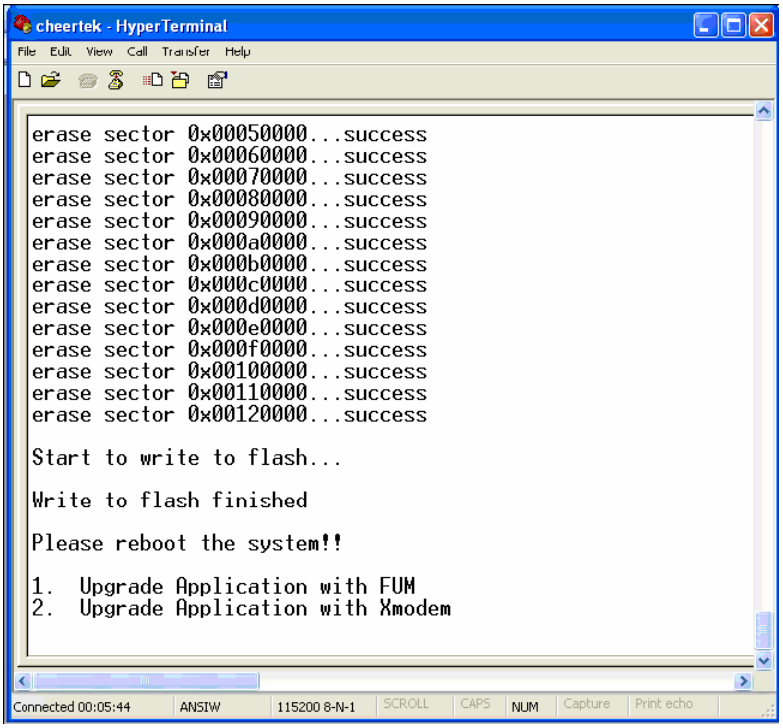


Figure 12. Capture of End of The Sending Process

11. For sending second program file, the Software Updating Procedure must be repeated from the step **X**. Select the "Filename **xxxx**_slot2.img" using "Browse".
12. After sending the second program file, the Software Updating Procedure will be succesful.

Note: After the File Sending Process,
1. Upgrade Application with FUM
2. Upgrade Application with Xmodem, options must be seen.

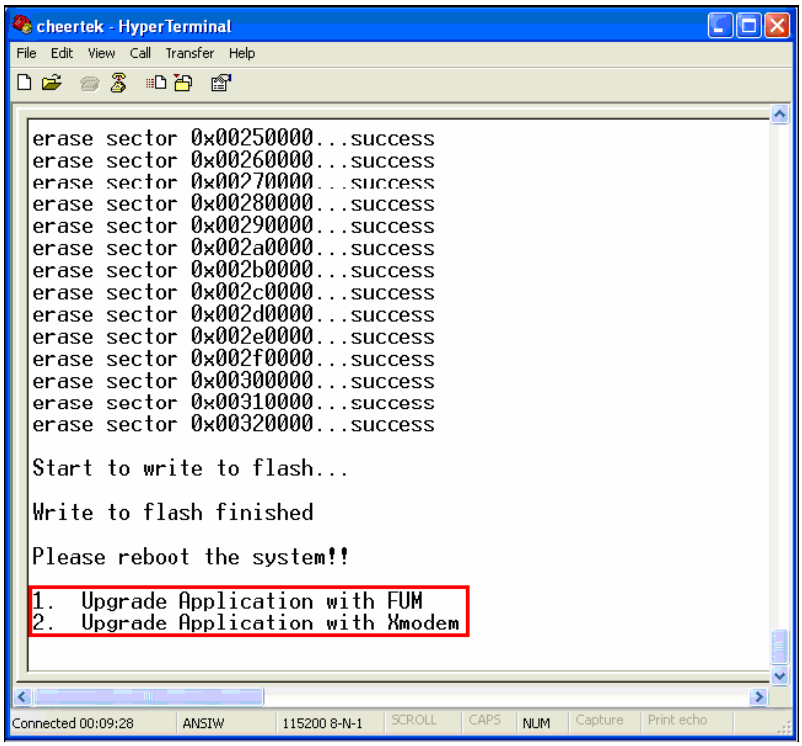


Figure 13. End of The Sending Process

Checking Of The New Software

1. Turn off and on the TV.
2. Enter the “Setup” submenu in the “DTV Menu”.
3. Choose the “Configuration” option.
4. For controlling new software, check the “Receiver Upgrade” option.

2..2 MB45 Digital Software Update From USB

Software upgrade is possible via USB disk by folowing the steps below.

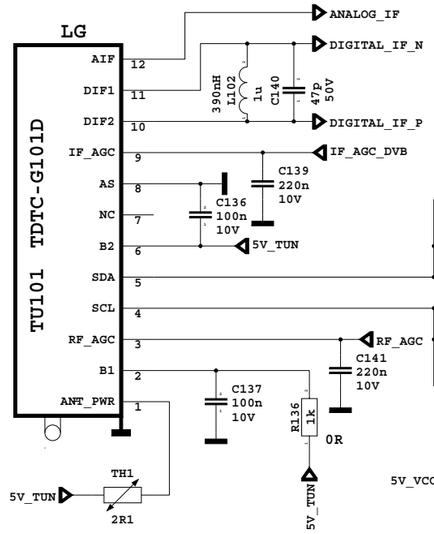
1. Copy the bin file, including higher version than the software loaded in flash, into the USB flash memory root directory. This file should be named up.bin.
2. Insert the USB disk.
3. Digital module performs version and CRC check. If version and CRC check is successful, then a message prompt appears to notify user about new version. If the user confirms loading of new version, upgrade.bin file is written into flash
unused slot.
4. Digital module disables the previous software in the flash and then a system reset is performed.
5. After the reset, digital module starts with new software.

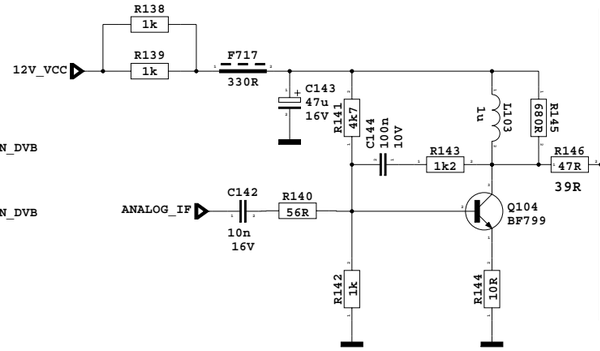
Revert operation:

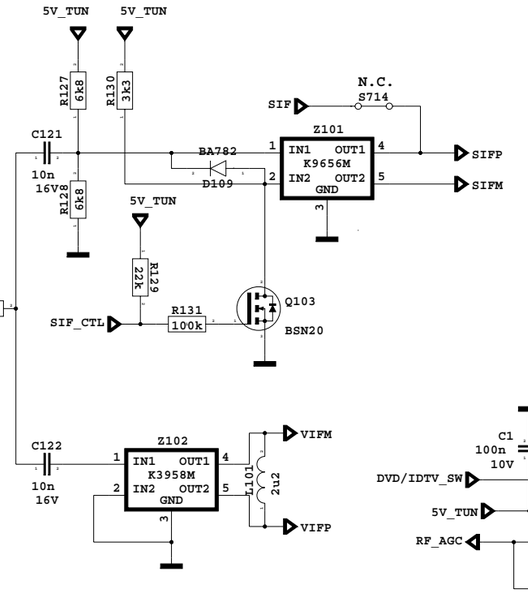
With revert operation, it is possible to *downgrade* the software.
Revert operation is very similar to upgrade process. In the revert operation, file name should be f_up.bin. Also user confirmation is not asked.

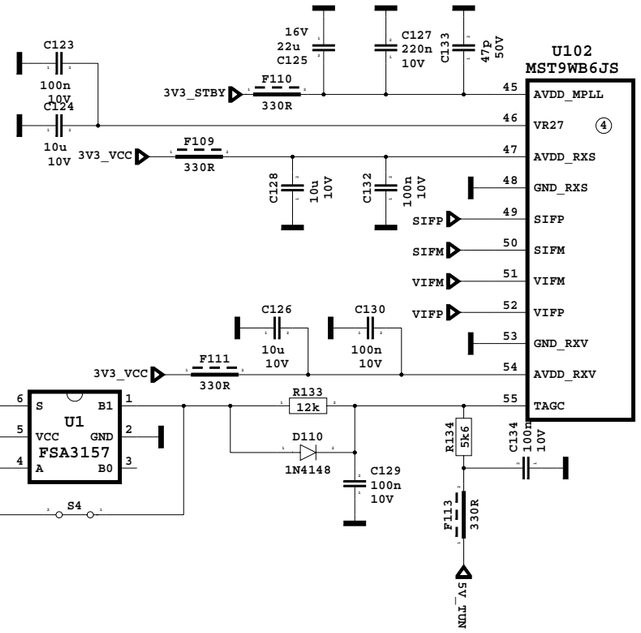
1. Copy the bin file into the USB flash memory root directory. This file should be named force_upgrade.bin.
2. Insert the USB disk.
3. A lower version than the software in flash can be loaded with revert operation. Digital module performs only CRC check. If CRC check is successful, then force_upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash.
5. A message prompt is displayed to notify user about end of revert process.
6. Power off/on is required to start digital module with the new software.

For controlling new software, check the “Receiver Upgrade” option.

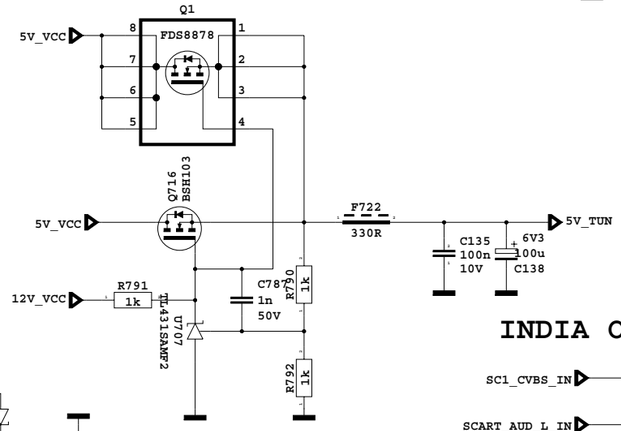




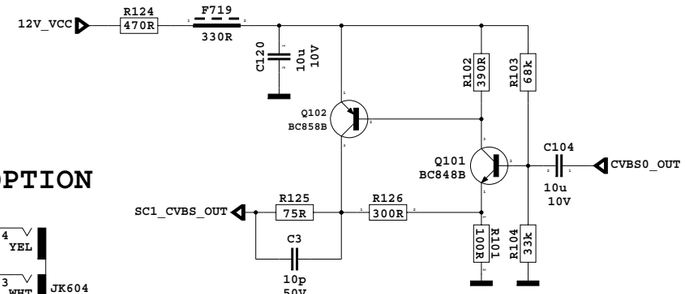




SCART VIDEO OUTPUT AMPLIFIER

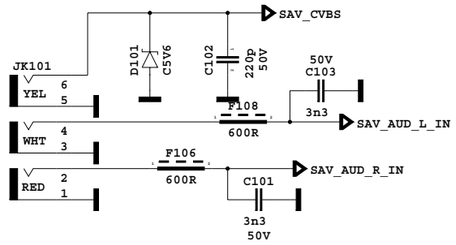


INDIA OPTION

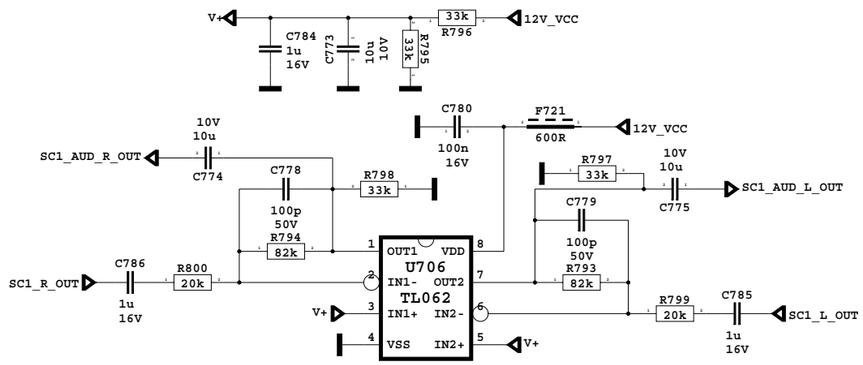


VGA INPUT

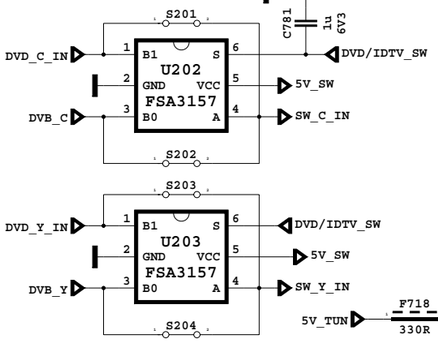
SIDE AV INPUT

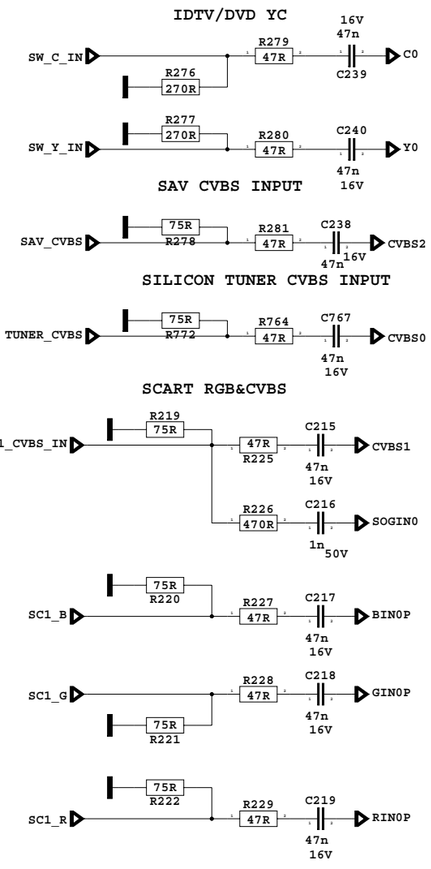


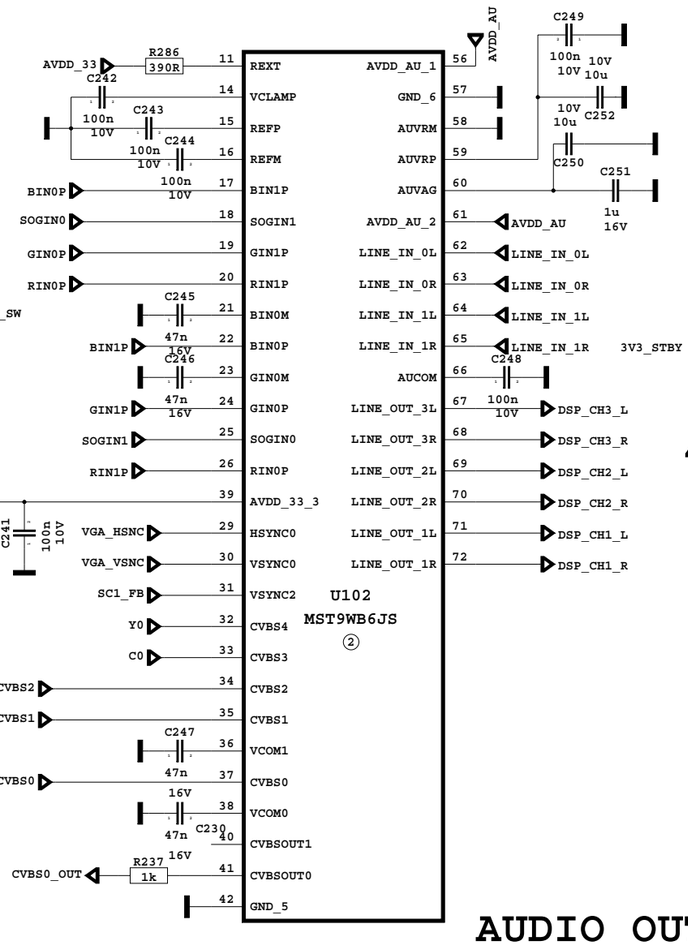
PRE-AMP for SCART



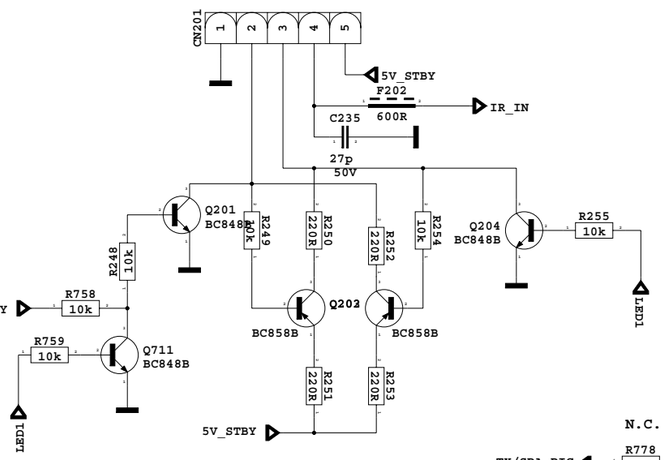
VIDEO INPUTs

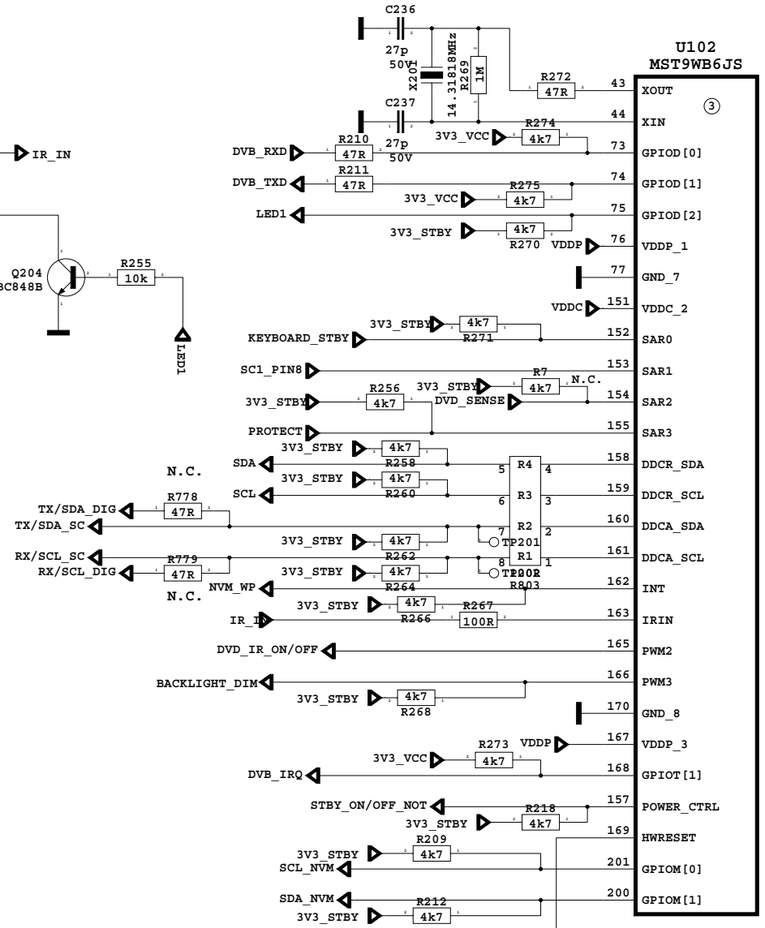




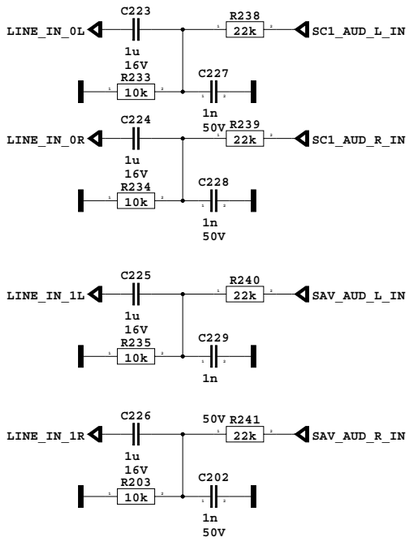


LED

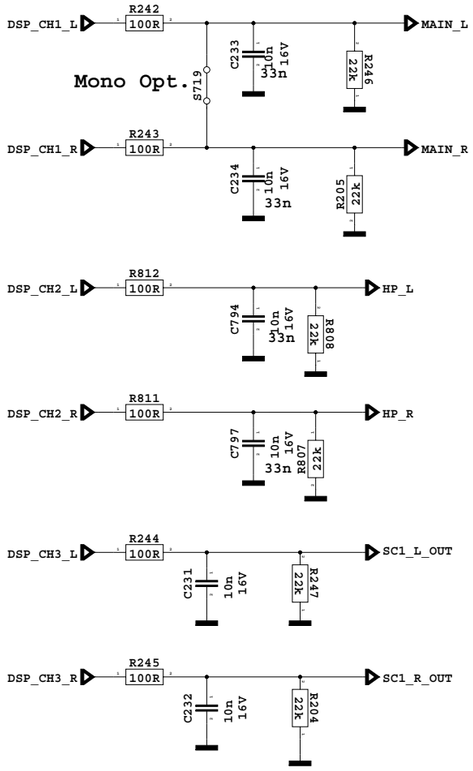


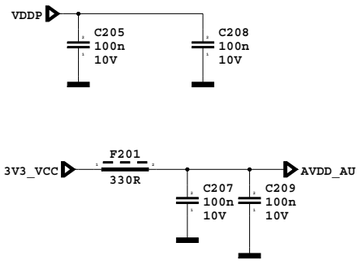


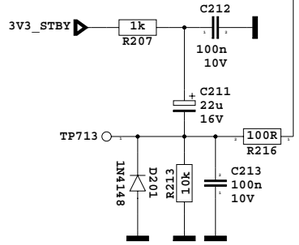
AUDIO INPUTs

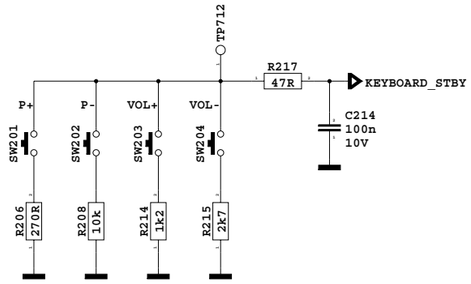


AUDIO OUTPUTs

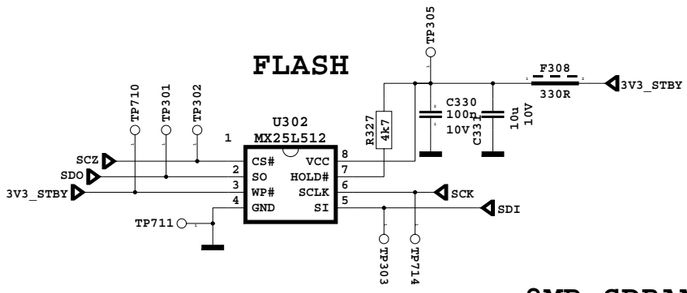


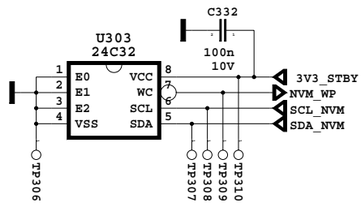


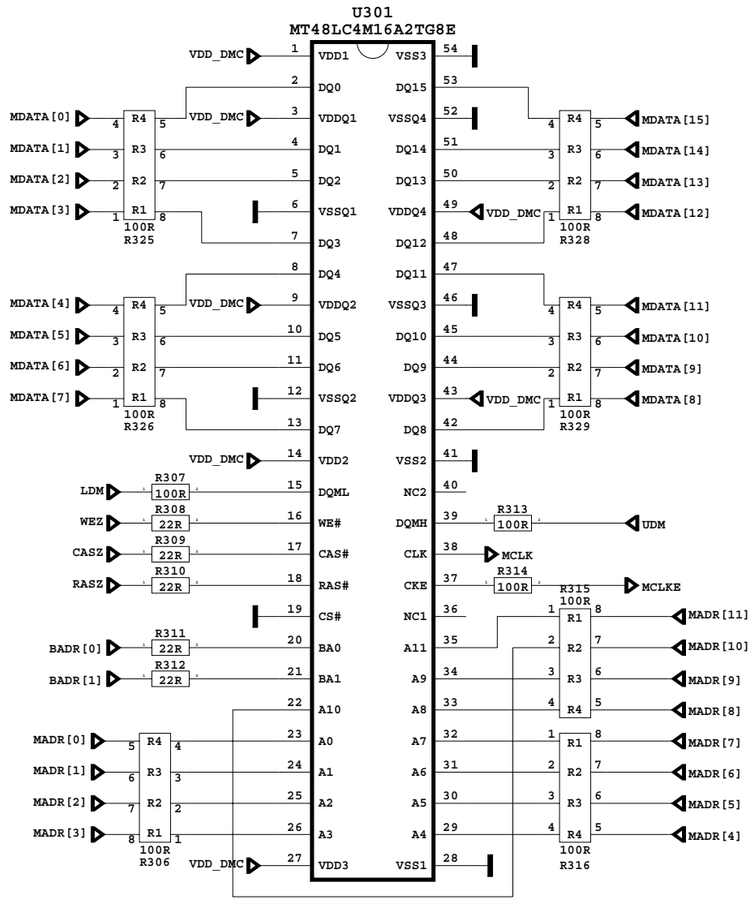


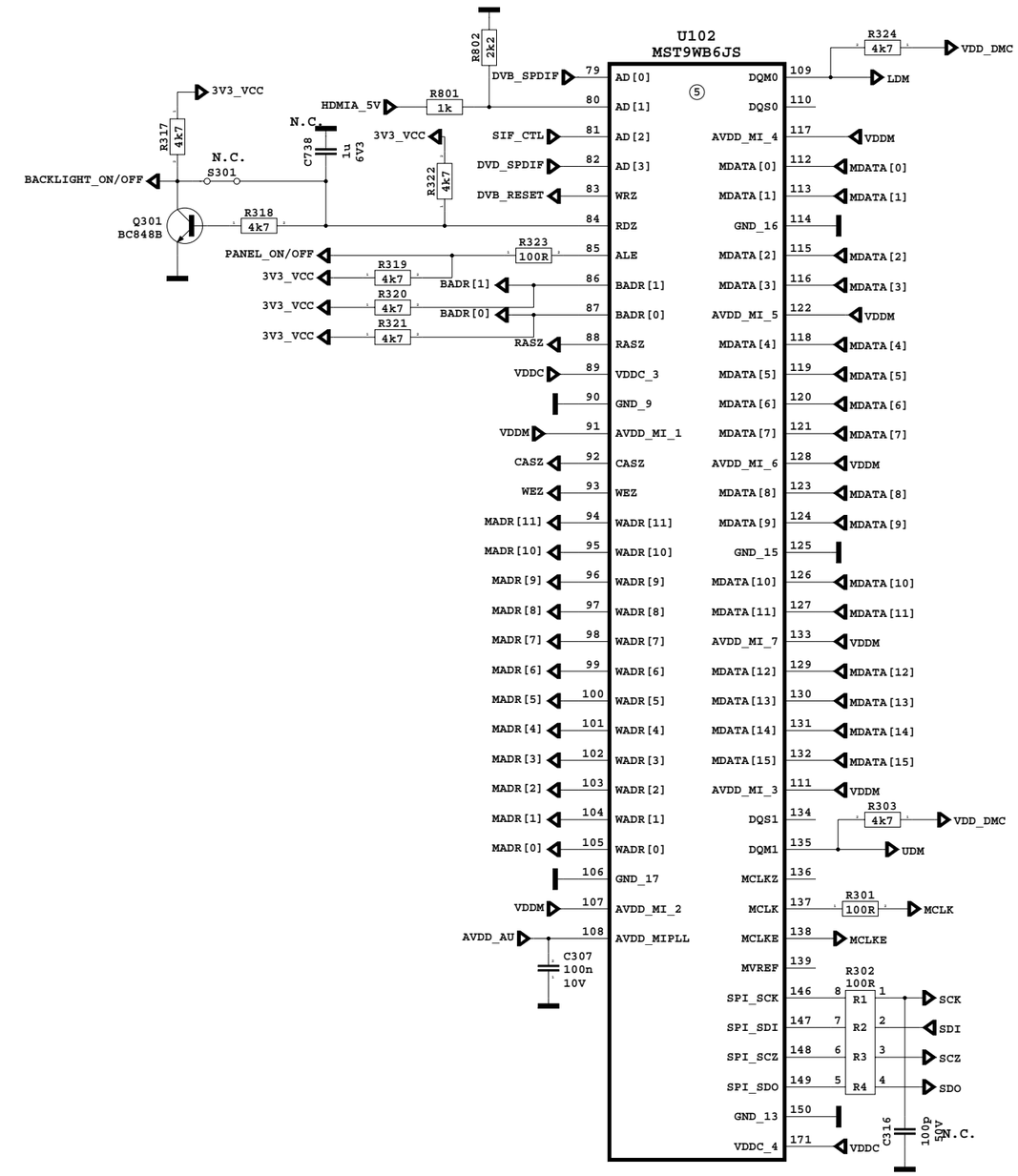


VESTEL	PROJECT NAME : 17mb45-3	A3
SCH NAME :A/V INTERFACE		SHEET:2 OF:8
DRAWN BY :ULAS DERELI		4-28-2008_15:57

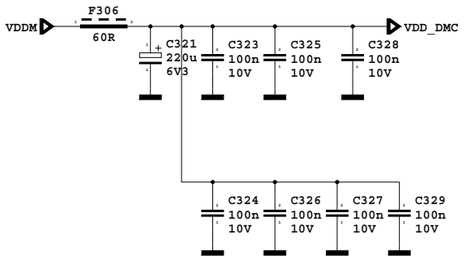


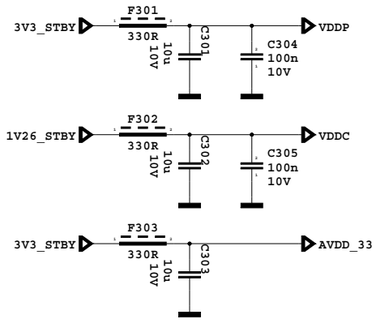


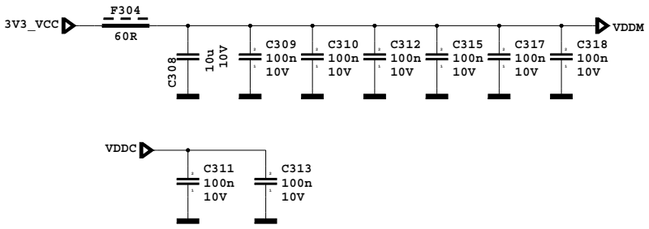




WARNING!!!DON'T USE VIA FOR MCLK AND DATA SIGNALS

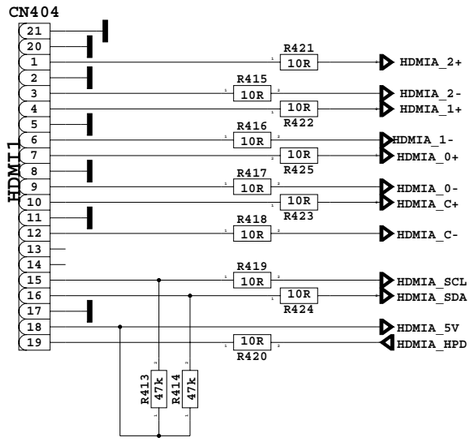


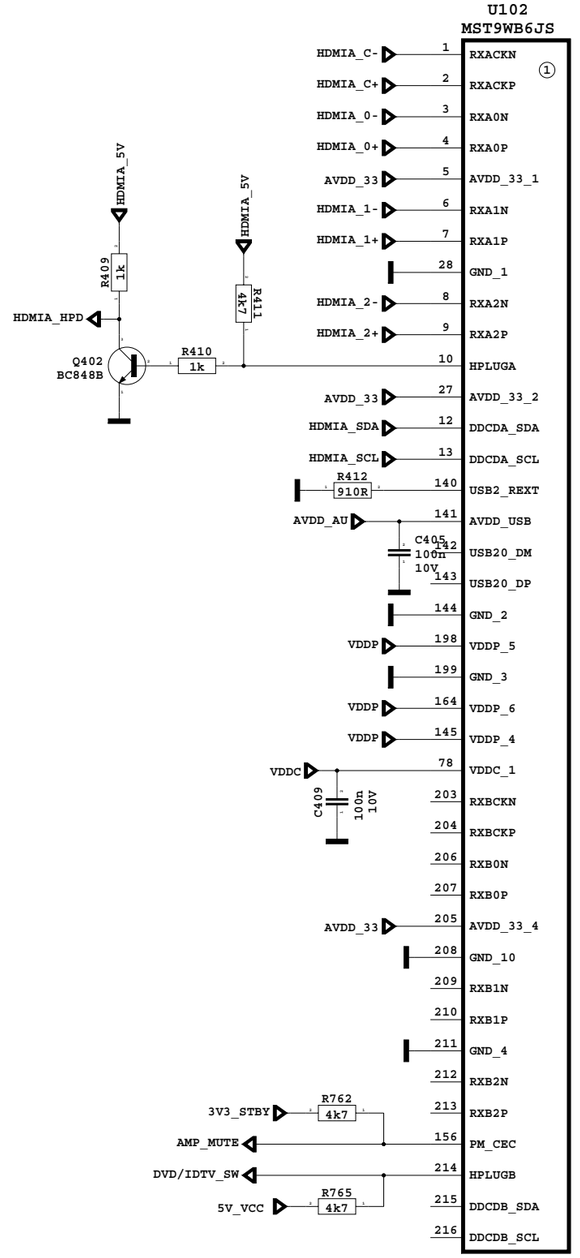


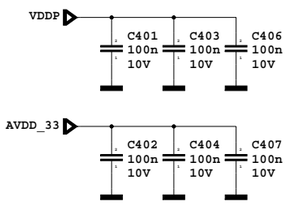


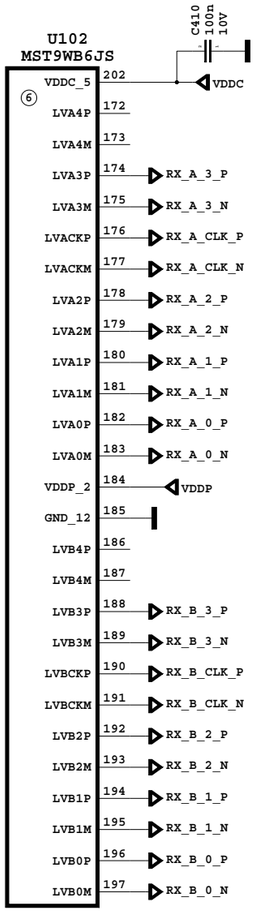
VESTEL	PROJECT NAME : 17mb45-3	A3
SCH NAME :MEMORY INTERFACE		SHEET:3 OF:8
DRAWN BY :ULAS DERELI		4-28-2008_15:57

HDMI

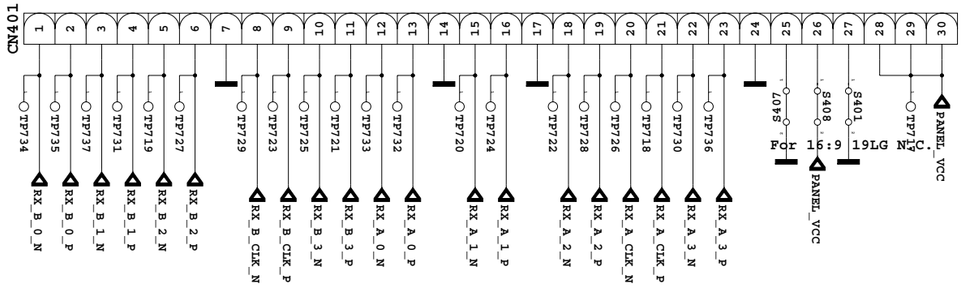


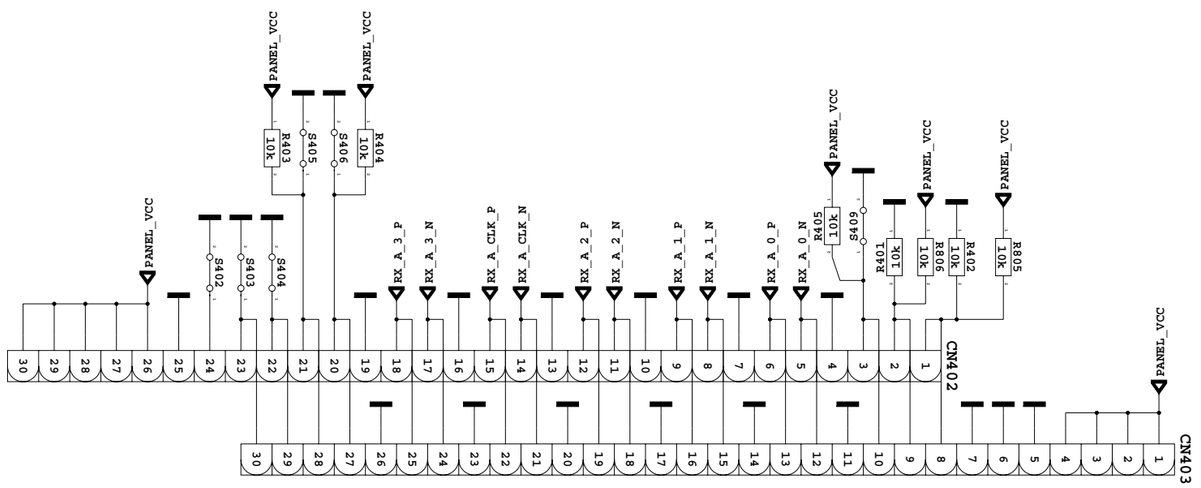






DUAL LVDS OUTPUT SOCKET





SINGLE LVDS OUTPUT SOCKET

VESTEL	PROJECT NAME : 17mb45-3	A3
SCH NAME :HDMI&LVDS OUT	SHEET:4	OF:8
DRAWN BY :ULAS DERELI	4-28-2008_15:57	

CHEERTEK

MPEG DECODER

U503
CT216T-R

FUM Interface (bottoma 2.54X2.54 yerlestirilecek)

CI CONTROL SIGNALS

U502 SDRAM
MT48LC4M16A2TG8E

DVB RESET

SERIAL FLASH

U501
MX25L512

MPEG DEC TS OUTPUT

MPEG DEC TS INPUT

RAM DATA BUS

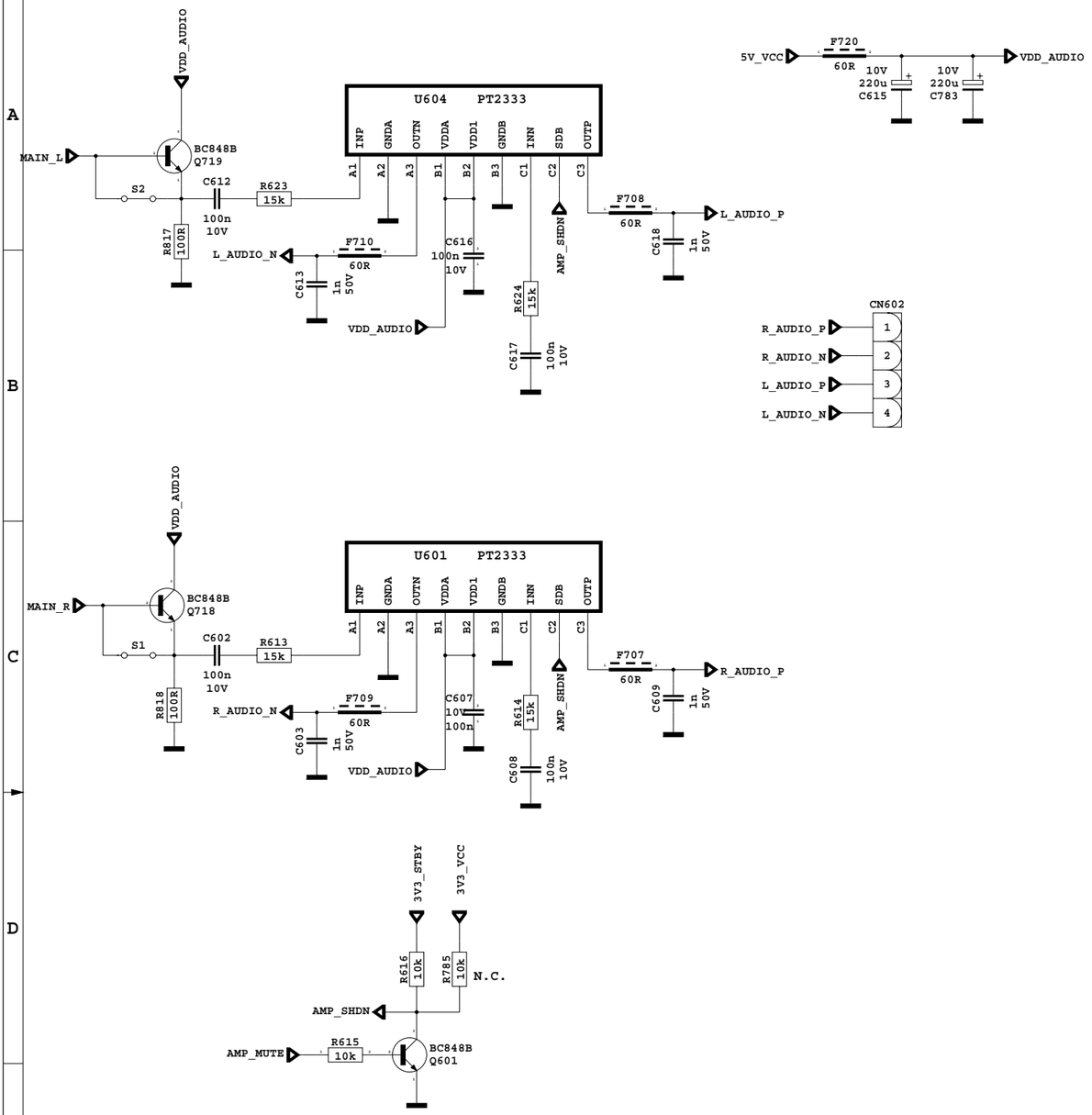
RAM ADDRESS BUS

CI ADDRESS BUS

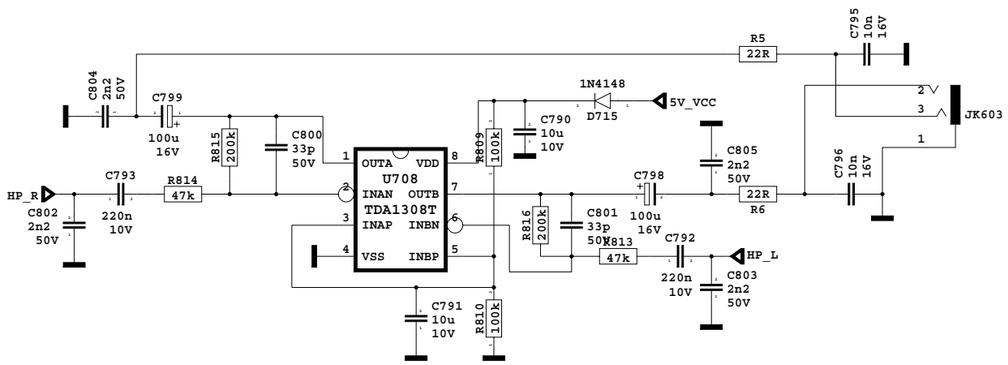
CI DATA BUS

Y/C Video Outputs ==>

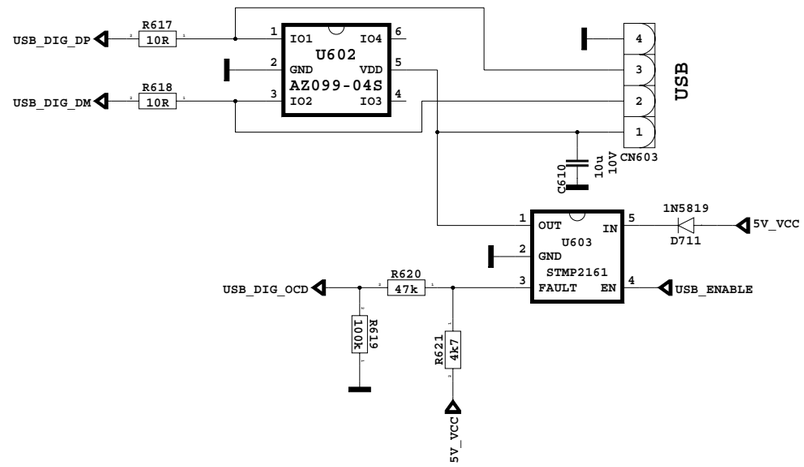
VESTEL	PROJECT NAME : 17mb45-3	A3
SCH NAME :DVB MPEG DECODER & SDRAM		SHEET:5 OF:8
DRAWN BY :ULAS DERELI		4-28-2008_15:57



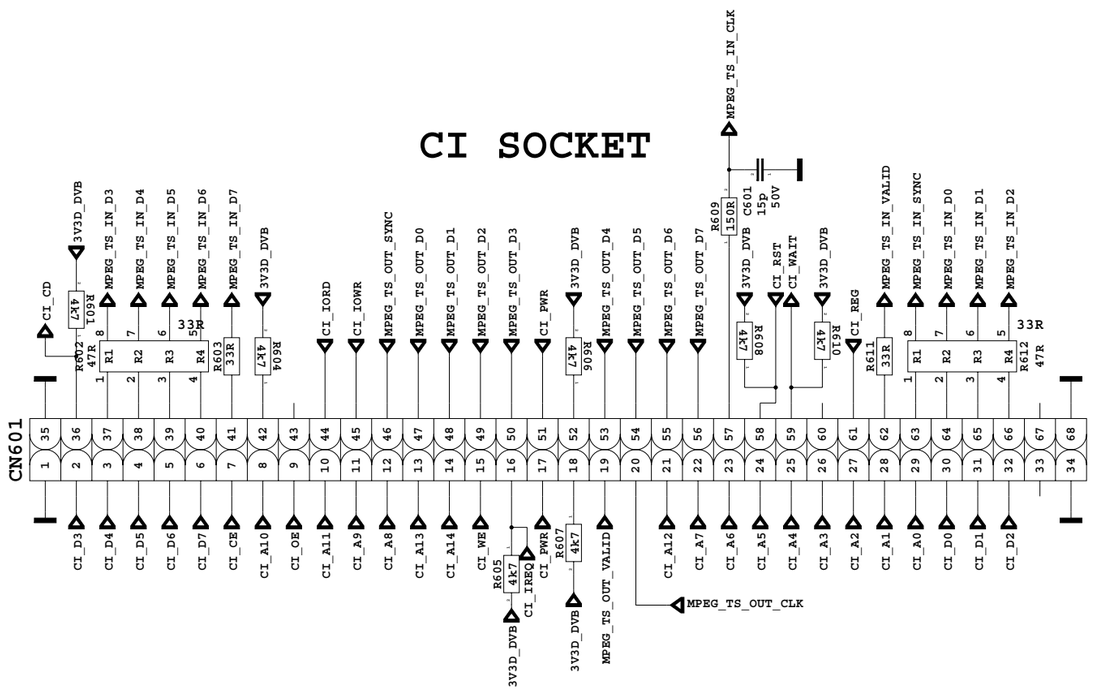
HEADPHONE AMPLIFIER



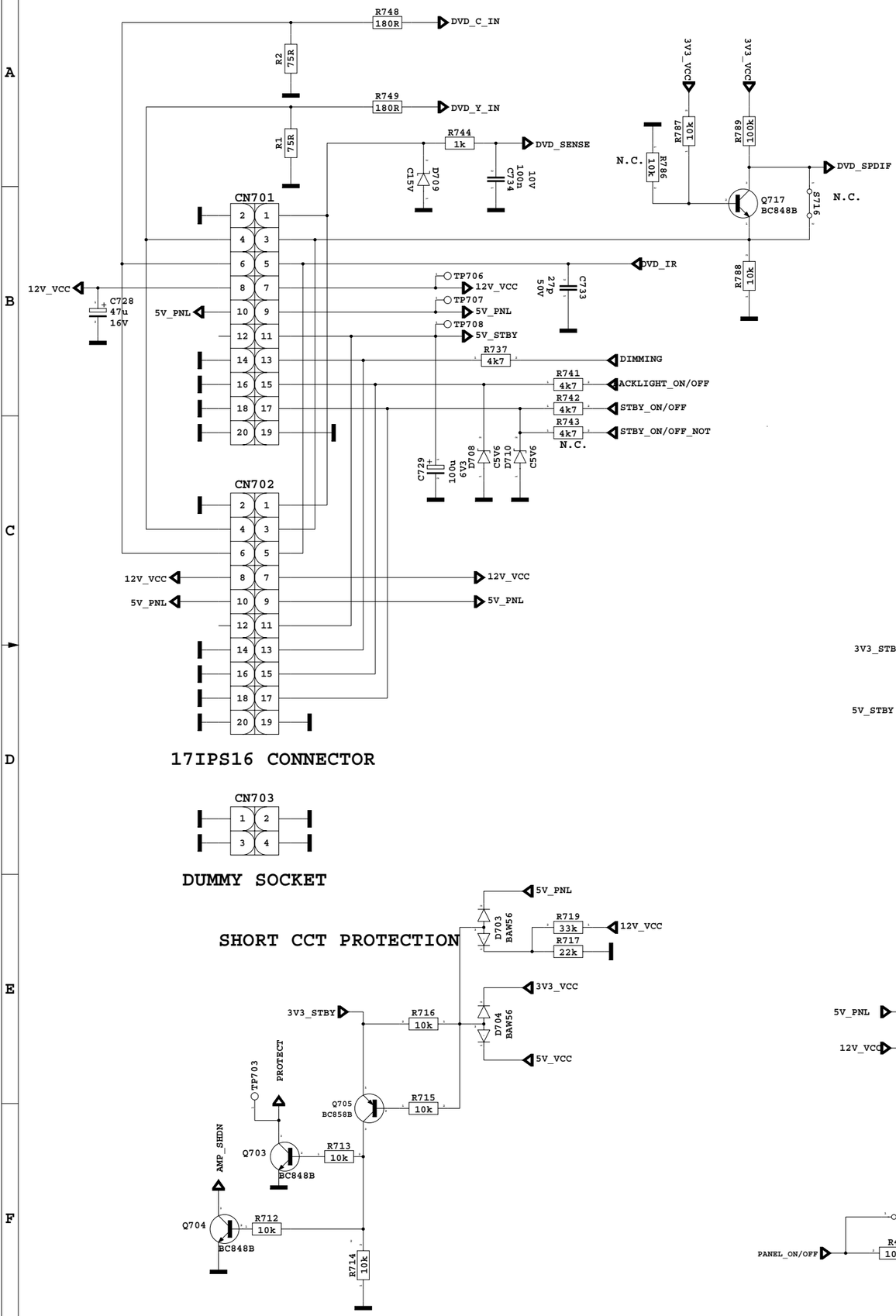
USB INTERFACE



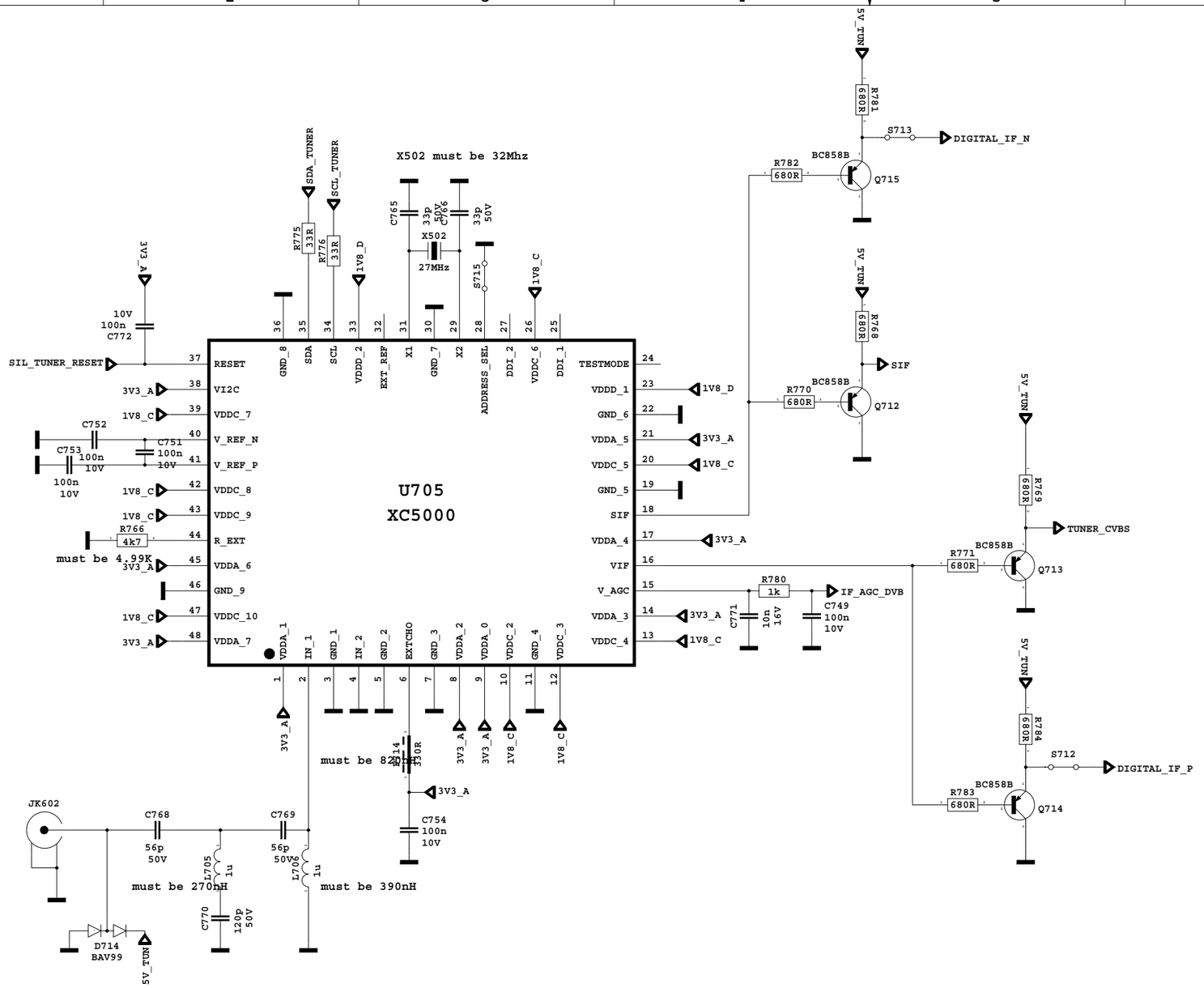
CI SOCKET

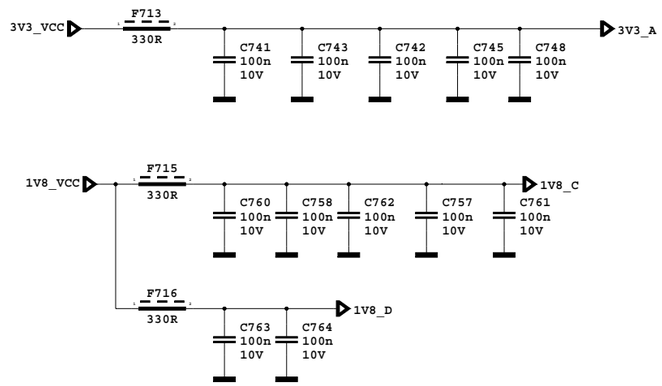


VESTEL	PROJECT NAME 17mb45-3	A3
SCH NAME :AUDIO AMP & CI & DIG.USB	SHEET:	OF:
DRAWN BY :ULAS DERELI	3-27-2008_13:22	



VESTEL	PROJECT NAME : 17mb45-3	A3
SCH NAME :POWER		SHEET:7 OF:8
DRAWN BY :ULAS DERELI		4-28-2008_15:57





VESTEL	PROJECT NAME : 17mb45-3	A3
SCH NAME :SILICON TUNER	SHEET:8 OF:8	
DRAWN BY :ULAS DERELI	3-27-2008_13:22